Single Line-of-Sight (SLOS) Imagers – Progress & Plans

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T. Hilsabeck, J. Kilkenny, D. Morris — GENERAL ATOMICS

M. Chung — TMC² LLC

J. Hares, T. Dymoke-Bradshaw — Kentech Instruments Ltd.

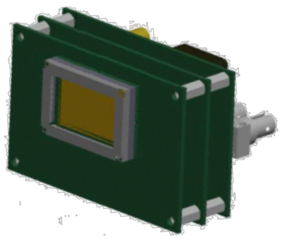
P. Bell, J. Celeste, A. Carpenter, M. Dayton, D. Bradley — Lawrence Livermore National Laboratory

G. Rochau, J. Porter, M. Sanchez,
L. Claus, G. Robertson, Q. Looker — Sandia National Laboratories

SLOS imaging is key to national strategy and transforms capability across ICF and the Science Campaigns

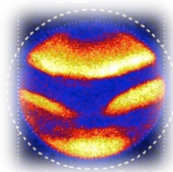
FY14	FY15	FY16	FY17	FY18		FY19
2 Fm, 1.5ns	8 Fm, 2ns (interlaced)	4 Fm, 1.5ns Low-E, e-	8 Fm, 1.5 ns (interlaced)	8 Fm, 1ns	8 Fm, 2 ns (interlaced) 20-40 keV	16 Fm, 1 ns (interlaced)

Key Direct Sensor Applications

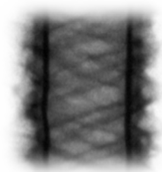


1-2 ns

LEH imaging (Z & NIF)

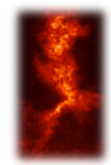


Backlighting (Z)

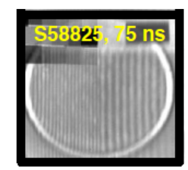


Opacity (Z)

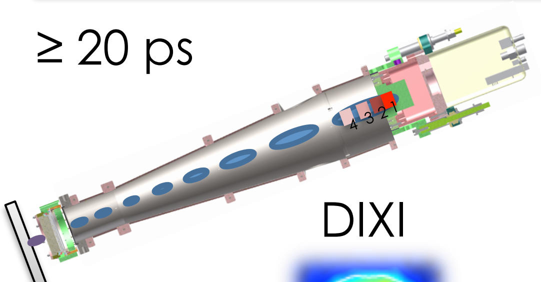
K-α Imaging (Z)



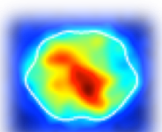
Strength (NIF)



≥ 20 ps

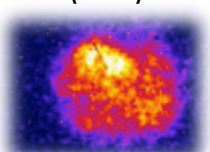


DIXI

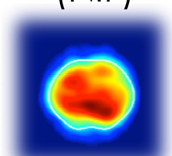


Key Pulse-Dilation Applications

SLOS-1
Pinhole
(NIF)

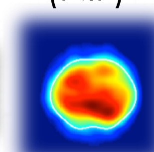


SLOS-2
KB
(NIF)



SLOS-3
Spectra (Z)

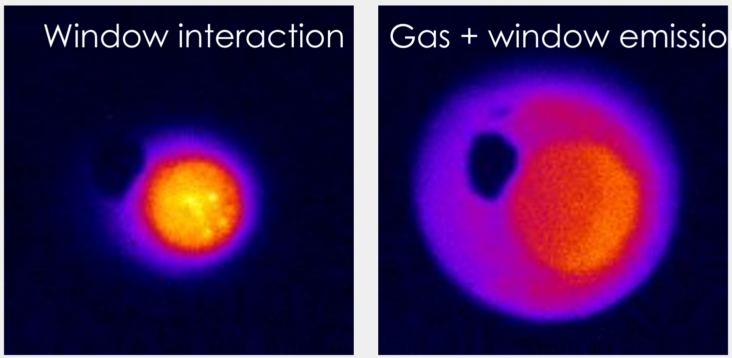
Wolter (NIF)

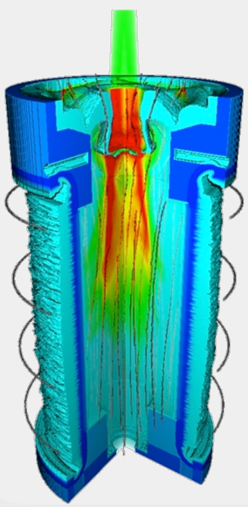


Multi-frame hCMOS imagers have recently been deployed for gated imaging on both Z and NIF

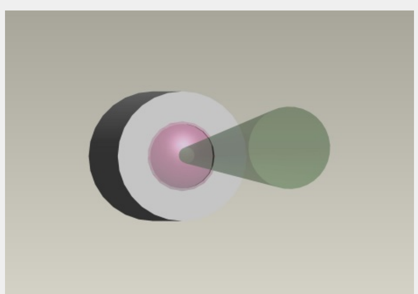
MagLIF laser preheat on Z*

9 ns gate separated by 10 ns



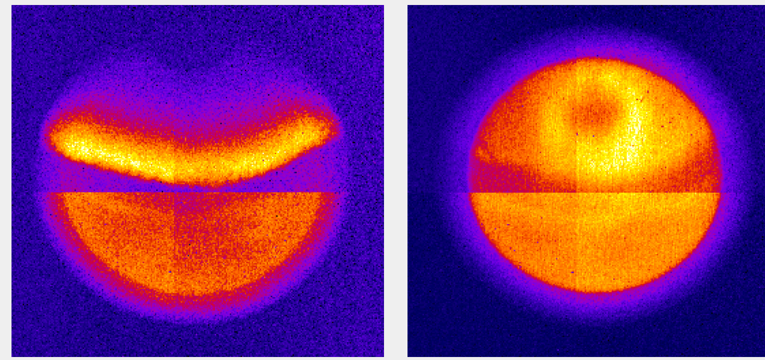


Camera View of LEH

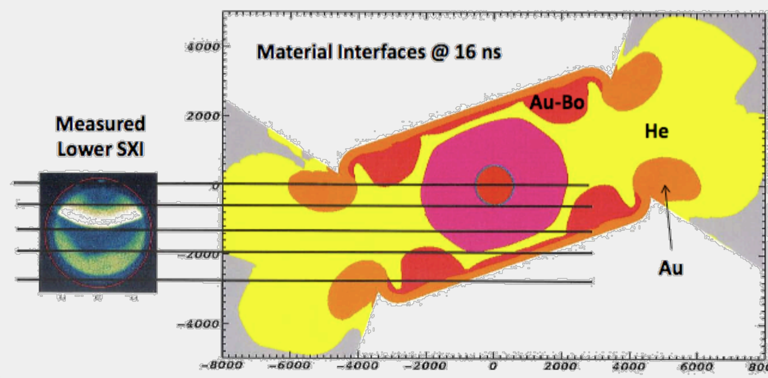


LEH imaging on NIF**

2 ns gate separated by 4 ns



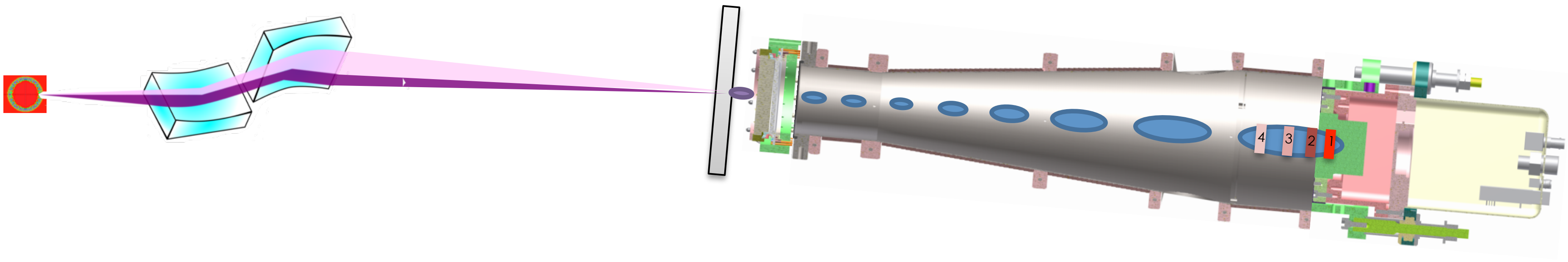
Camera View of LEH



*Porter (SNL) et al.

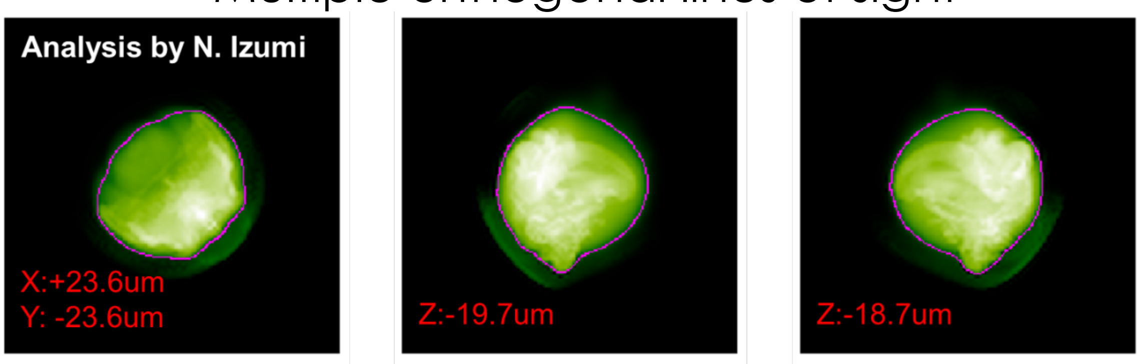
**Chen (LLNL) et al.

Pulse-dilation SLOS with reflective x-ray optics solves high spatial and temporal resolution image problem



<u>Three orthogonal LOS can theoretically provide some 3-D information*</u>

Multiple orthogonal lines of sight



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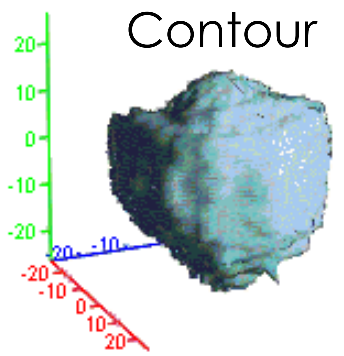
Reconstructed 3-D Contour

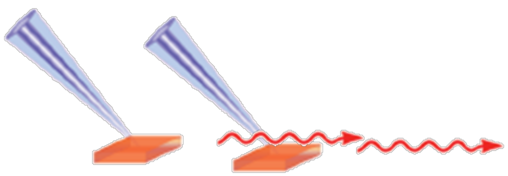


*Izumi (LLNL) et al.

High energy, single line-of-sight gated cameras are needed for face-on point-projection radiography on NIF

Backlighter

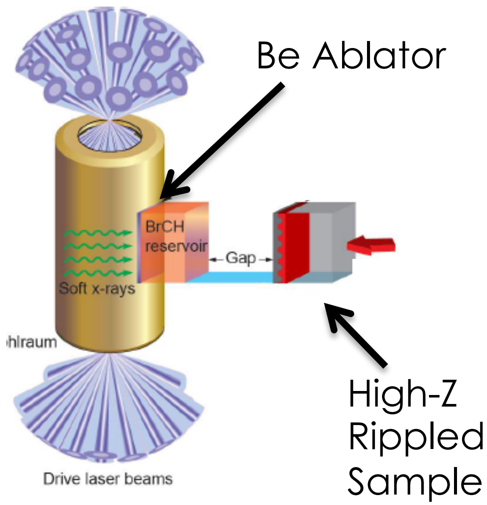
Short-pulse
Laser beams

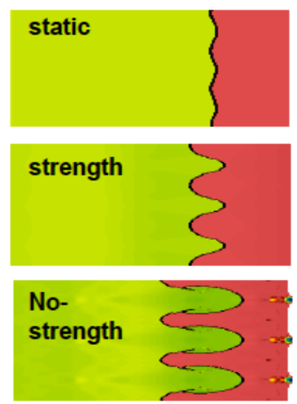


17-40 keV
X-rays

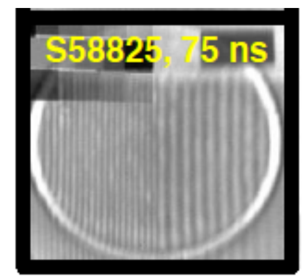
- Optimal energy depends on Z and thickness

RT Strength Platform





Face-on Radiography



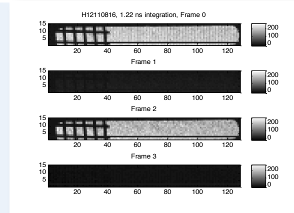
Face-on radiography

Detector Requirements

- 2mm x 4mm FOV at target
- <10 um/pixel at tcc
- QE of 50% at 17-22 keV
- 2-4 frames
- 5-20 ns frame separation
- ≥2 ns gate time
- Dynamic Range > 200

In the next 3 years, we will deploy a >1 MP hCMOS imager with 1 ns gate times over 8+ frames

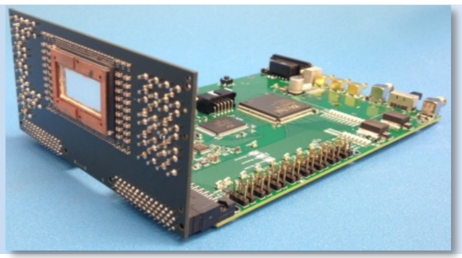
GRIFFIN
1.5ns, 4 Frames
15x128 pixels
350nm Sandia Process

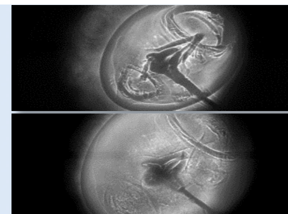


Calibration Mesh X-ray 1.5ns Images

FY13

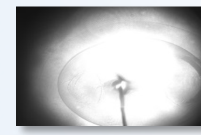
FURI
1.5ns, 2 Frames
448x1024 pixels
350nm Sandia Process





10ns Blast Wave Visible Images

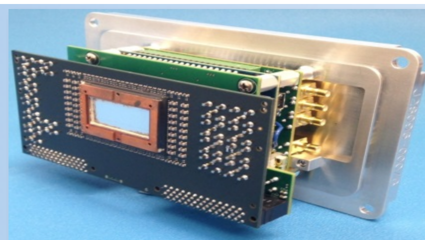
vs.

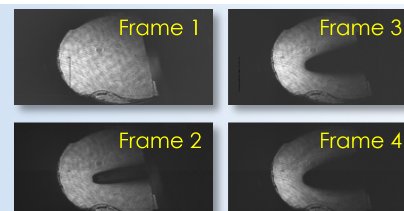


Commercial Double Exposed CCD

FY14

HIPPOGRIFF
2 ns, 2-8 Frames (Interlacing)
448x1024 pixels
350nm Sandia Process



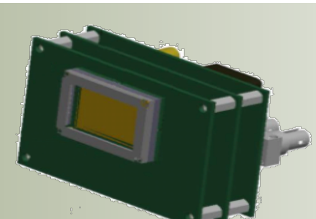


4ns Gas Cell Shadowgraphs

FY15

ICARUS
1.5ns, 4-16 Frames (Interlaced)
512x1024 pixels
350nm Sandia Process

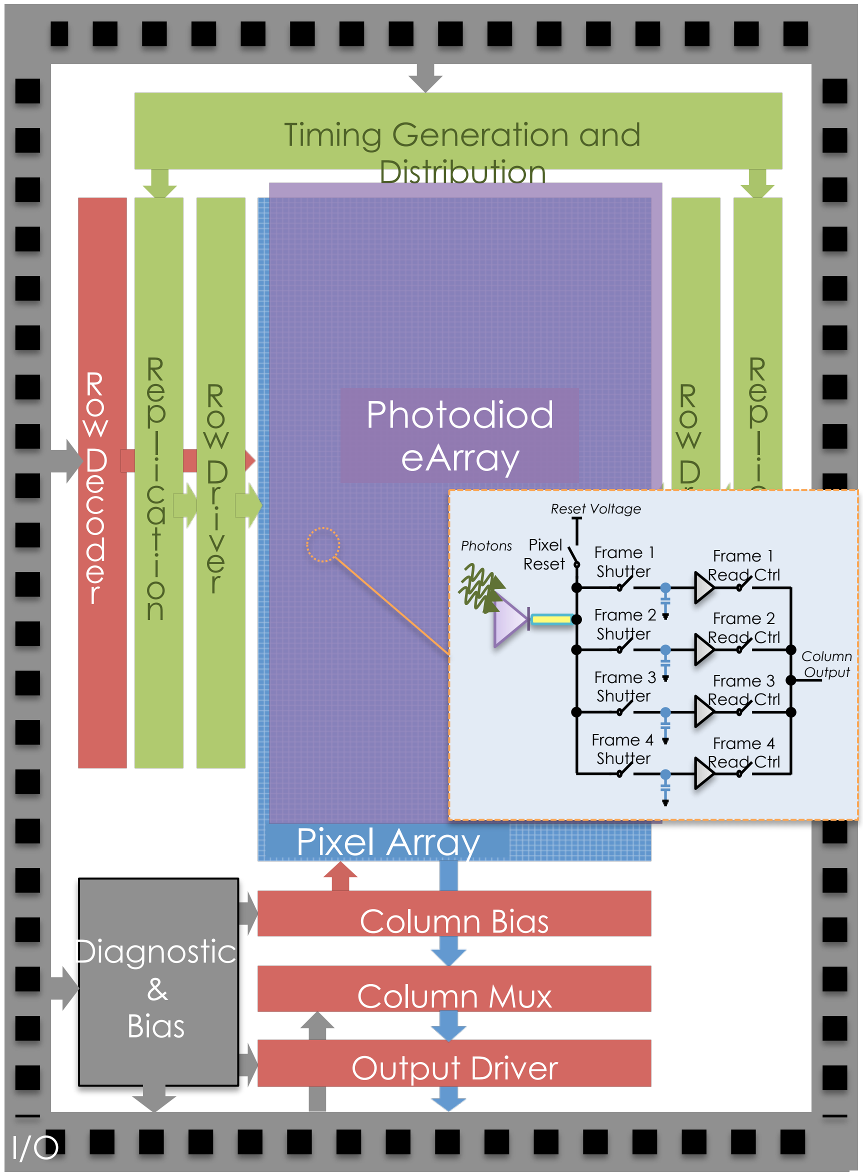
ACCA
1ns, 8 Frames
512 x 512 pixels (1-D tileable)
130nm IBM Process



FY16-18

UXI ROIC Architecture

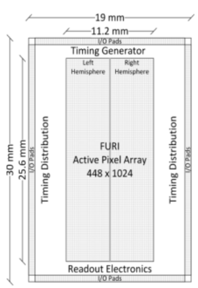
- Pixel Array
  - 2-4 Frame In Pixel Storage
  - Global Shutter
- Timing
  - High Speed Shutter & Pixel Control
  - Adjustable Shutter Timing 1-19ns
  - Adjustable Delay Between Shutters
- Readout
  - Random Access to Pixels (Region Of Interest)
  - Multiple Parallel Channels Of Image Data
- Photodiode
  - 0.7-6keV X-rays & 500-900nm Visible Light
- I/O and Support
  - Timing Signal Diagnostics

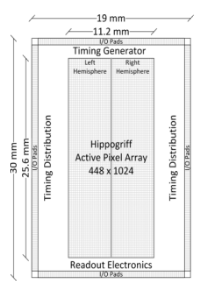


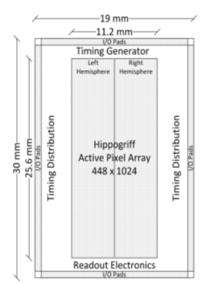
UXI Camera Designs Existing or in Progress

'High' Full Well Sensors

	Presently in Use		New Design
	Furi	**Hippogriff**	**Hippogriff 2**
Year	**FY14**	**FY15**	**FY17**
Min. Gate	**~1.5 ns**	**~2 ns**	**~1.5 ns**
Frames	**2**	**2 (full-chip), 4 or 8 (interlaced)**	
Tiling Option	**No**	**No**	**TBD**
CMOS Process	**350 nm (SNL)**		
Pixels	**448 x 1024**		
Pixel Size	**25 μm x 25 μm**		
Capacitor Full Well	**1.5 million e$^-$**		

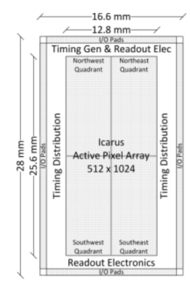


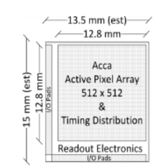




'Low' Full Well Sensors

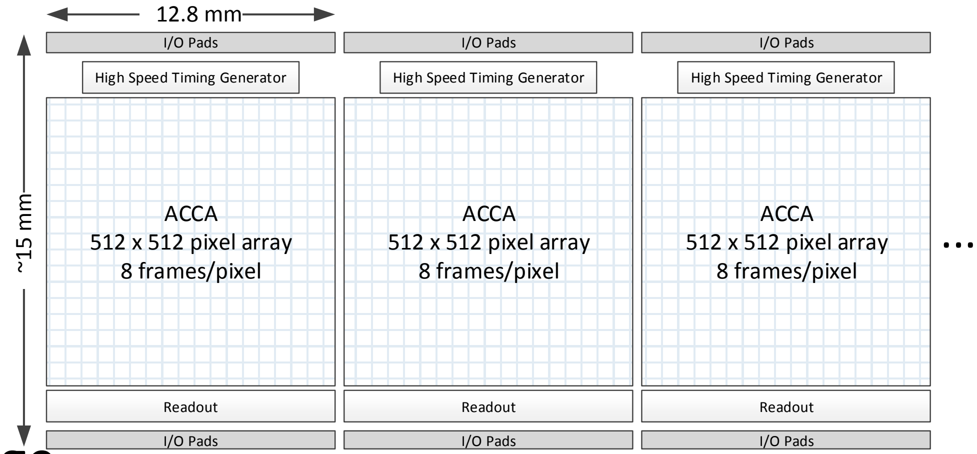
	Pulse Dilation	
	Icarus	**Acca**
Year	**FY16**	**FY18**
Min. Gate	**~1.5 ns**	**~1 ns**
Frames	**4**	**8**
Tiling Option	**No**	**Linear Tiling**
CMOS Process	**350 nm (SNL)**	**130 nm (IBM)**
Pixels	**512 x 1024**	**512 x 512**
Pixel Size	**25 μm x 25 μm**	
Capacitor Full Well	**0.5 million e$^-$**	





ACCA-The next generation burst mode hCMOS imager under development at SNL

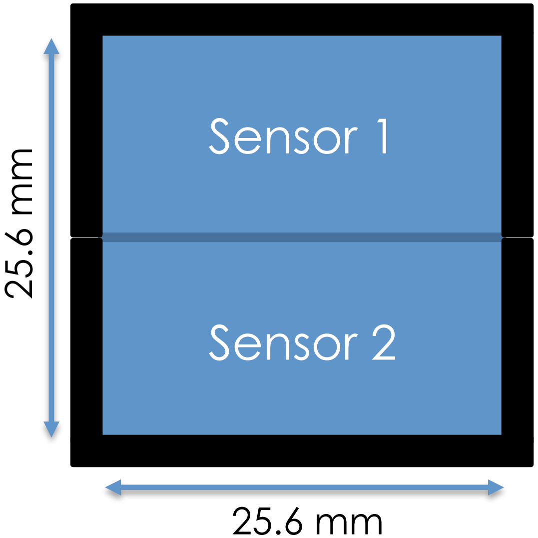
- **Specifications**
  - 512 x 512 pixel array
  - 8 frames per pixel
  - 1 ns integration time
  - 2 ns frame rate
  - 25 µm spatial resolution
  - Left/Right abutable design
  - 60 dB (1000:1) dynamic range
    - 500e- to 500k e-
  - Reduced readout dead-time
    - 1.45 ms per read-off of 512x512 pixels and 8 frames
      - Improvement from 135 ms on 1st generation imagers
    - 689, 8-frame movies per second in continuous read mode

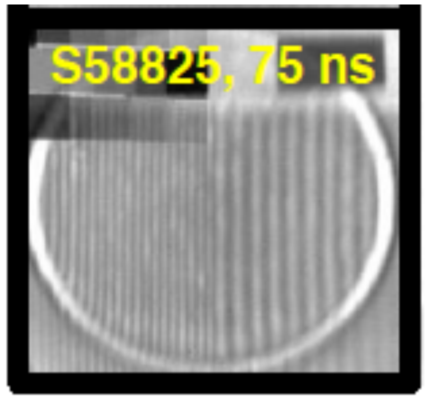


The ACCA architecture enables a scalable number of frames and form-factor

- **Innovations**
  - Leveraging higher density 130 nm technology node
    - Increased transistor density and metal interconnect layers enable significant design improvements
  - Left/Right 2-side abutment form factor
    - Infinite tiling in one direction
  - Differential CML H-tree timing distribution
    - Expect improved timing distribution uniformity
    - 2 global clocks distribute Pulse Width Modulation (PWM) encoded shutter information
  - In-pixel digital shutter generator converts the global clock PWM information to individual frame shutters
    - This architecture is scalable in number of frames while never requiring more than the 2 global clock signals to be distributed
- **Risks and mitigation strategy**
  - New technology (IBM 130nm CMOS8RF process)
    - Process leakage is worse with IBM than SNL's 350 nm CMOS7 process that our current ROICs are fabricated in
      - Increased readout speed to minimize leakage effects (1.45 ms)
      - Cool the device to 0 C
    - Bulk technology susceptibility to radiation
      - Test under radiation

GaAs diodes coupled to a Hippo-like ROIC with 50μm pixels could meet the needs for point-projection backlighting on NIF





ROIC (Hippogriff like)

- 50um pixels
- 512x512 pixels with 2 tiled sensors
- 2 frames or 4,8 frames interlaced
- ~2ns per frame
- Up to 6E6 e- per pixel per frame (~1200 photons at 22 keV in GaAs)

Detector

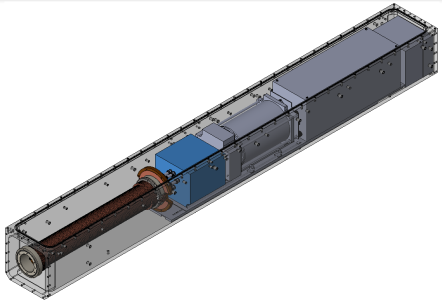
- 50um thick GaAs
- Photo-absorption > 50% at < 24 keV
- < 1 ns response time

Primary Challenges

- Pixelated GaAs arrays have been built before, but maybe not at this thickness
- Defects in GaAs need to be studied to determine yield (density of good pixels)
- Handling of potentially large currents needs to be studied
- ROIC needs to be re-designed for larger pixels and for 1-side abuttment
- Speed of ROIC needs to be studied with larger pitch and higher capacitance per frame

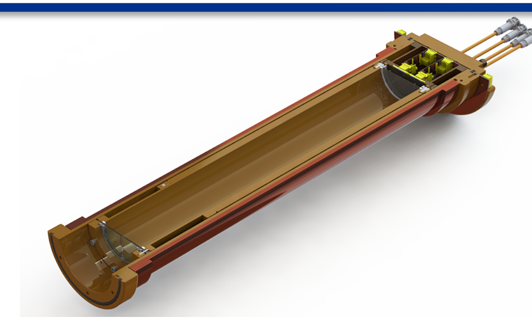
Integration of pulse-dilation, hybrid CMOS and x-ray optics staged over several years

- **SLOS1**

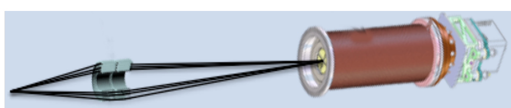


  - **8 frames in 200 ps – 1 ns**
  - **2 images from pinholes**
  - **1 Icarus sensor**

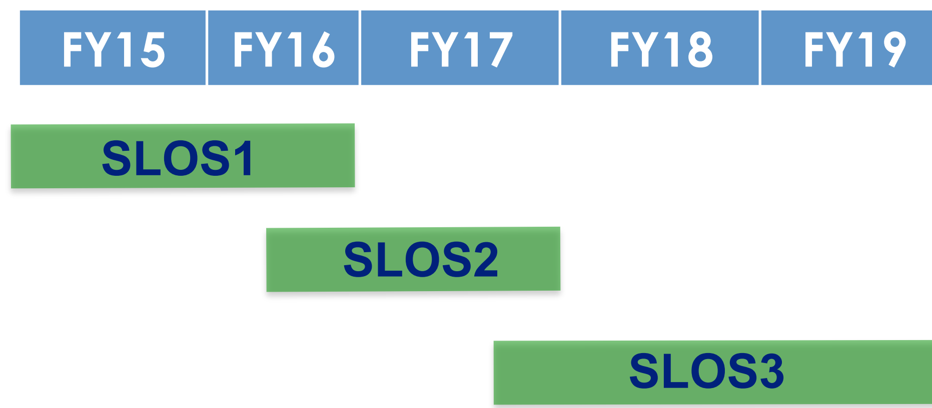
- **SLOS 2:**



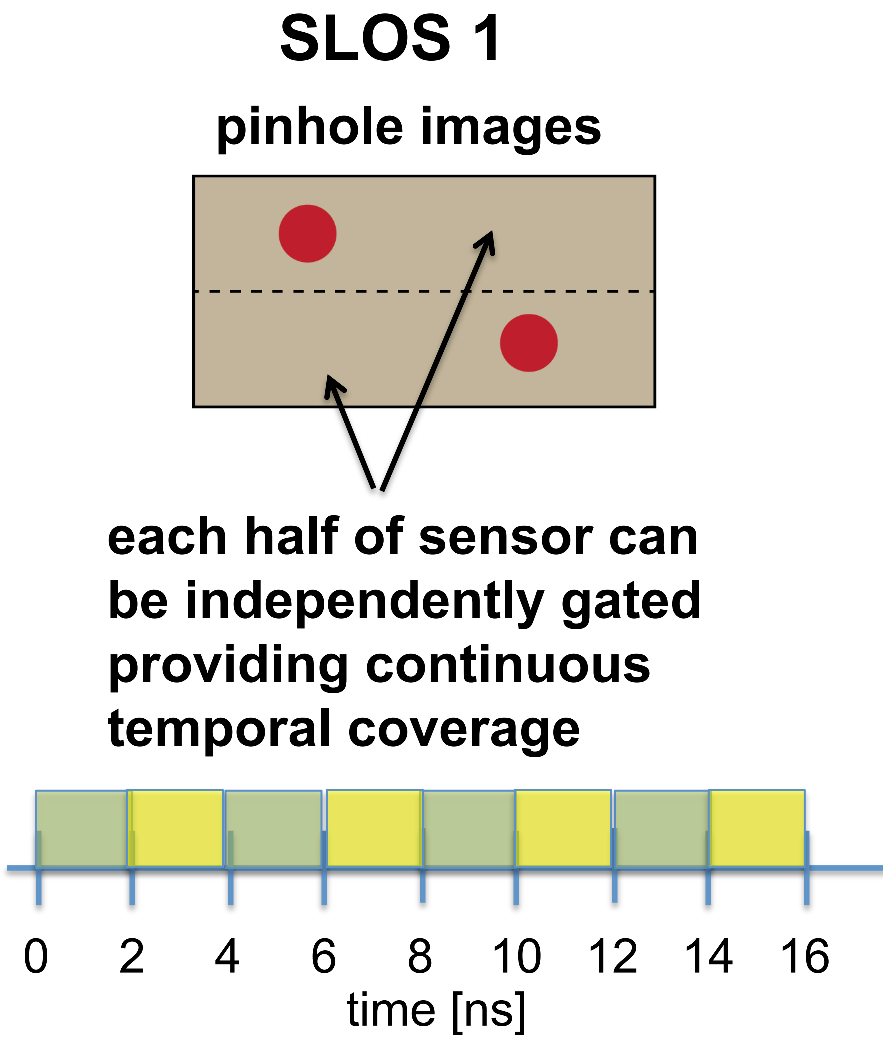
  - **16 frames in 400 ps – 2 ns**
  - **4 images from KB Optic**
  - **2 Icarus sensors**

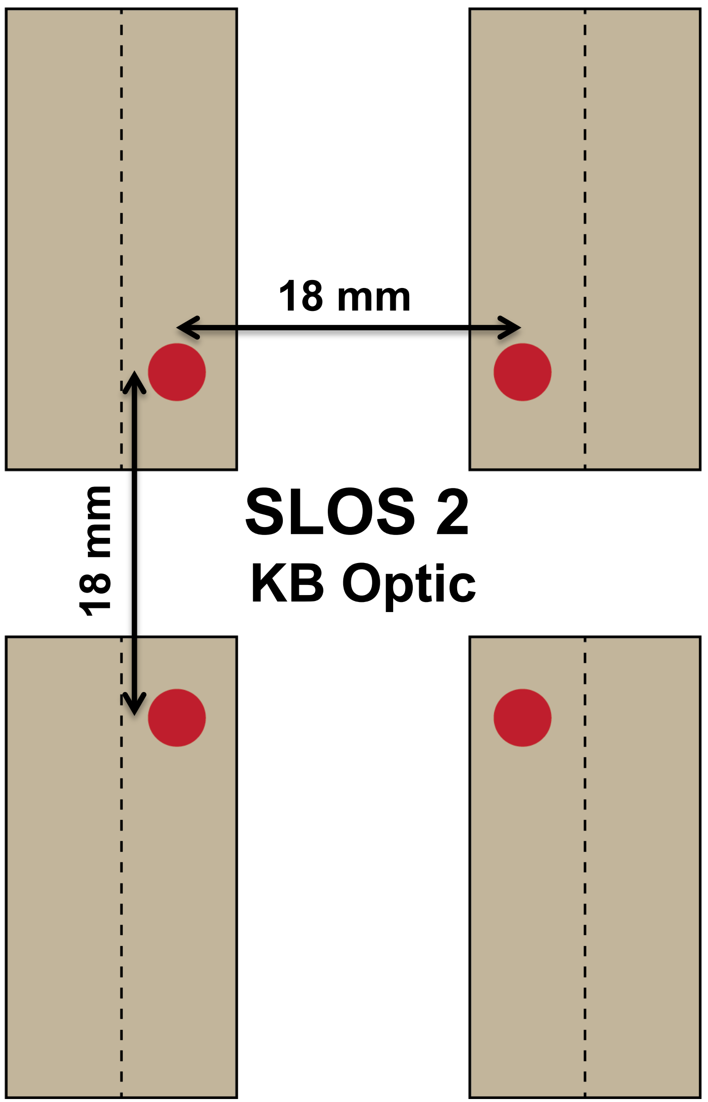


- **SLOS 3:**
  - **24 frames in 400 ps – 2 ns**
  - **3 images from Wolter**
  - **3 Acca sensors**



SLOS 1 prototype instrument to be fielded with pinholes
SLOS 2 will be designed to match KB Optic image layout



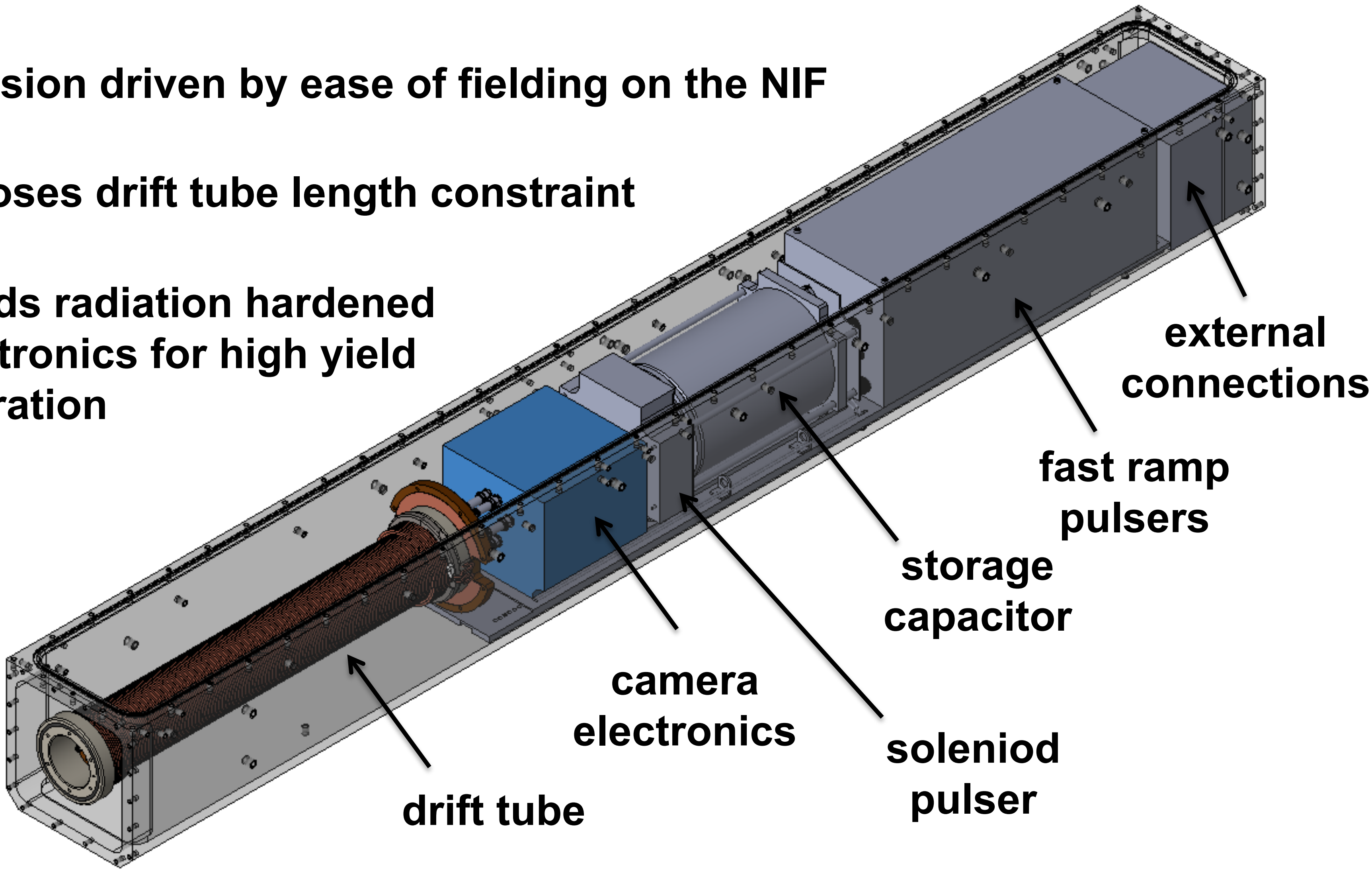


SLOS 1 is required to fit in a standard DIM airbox including all pulsers, electronics and energy storage for magnetic field

Decision driven by ease of fielding on the NIF

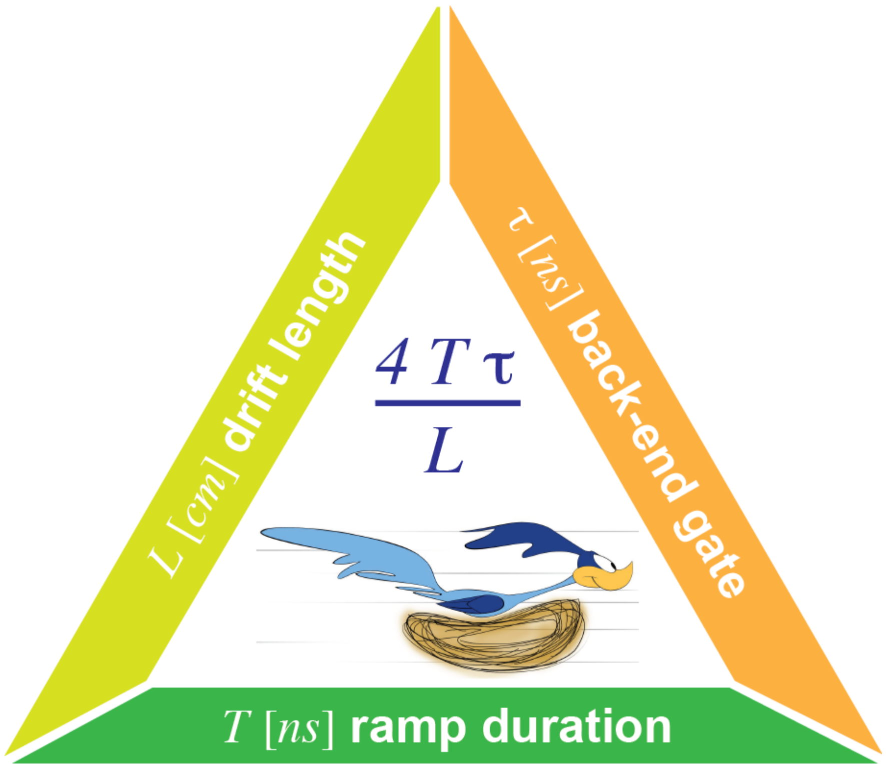
Imposes drift tube length constraint

Needs radiation hardened electronics for high yield operation



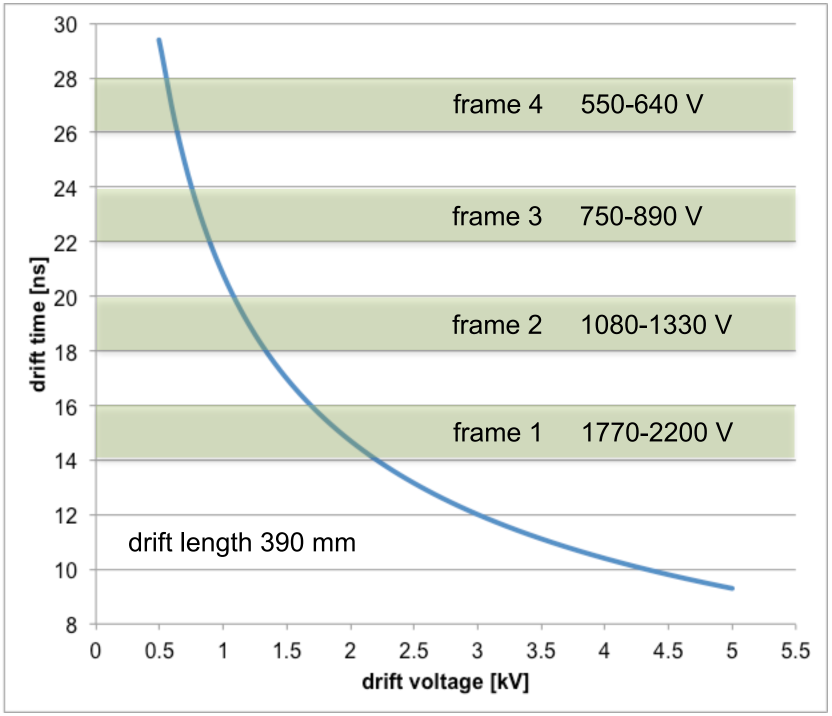
SLOS 1 performance parameters set by system contraints (DIM airbox length, CMOS gate time) and physics

Pulse-dilation Triangle



ramp duration = record length

assumes CMOS sensor 2 ns gate
& 2 ns interframe dark interval



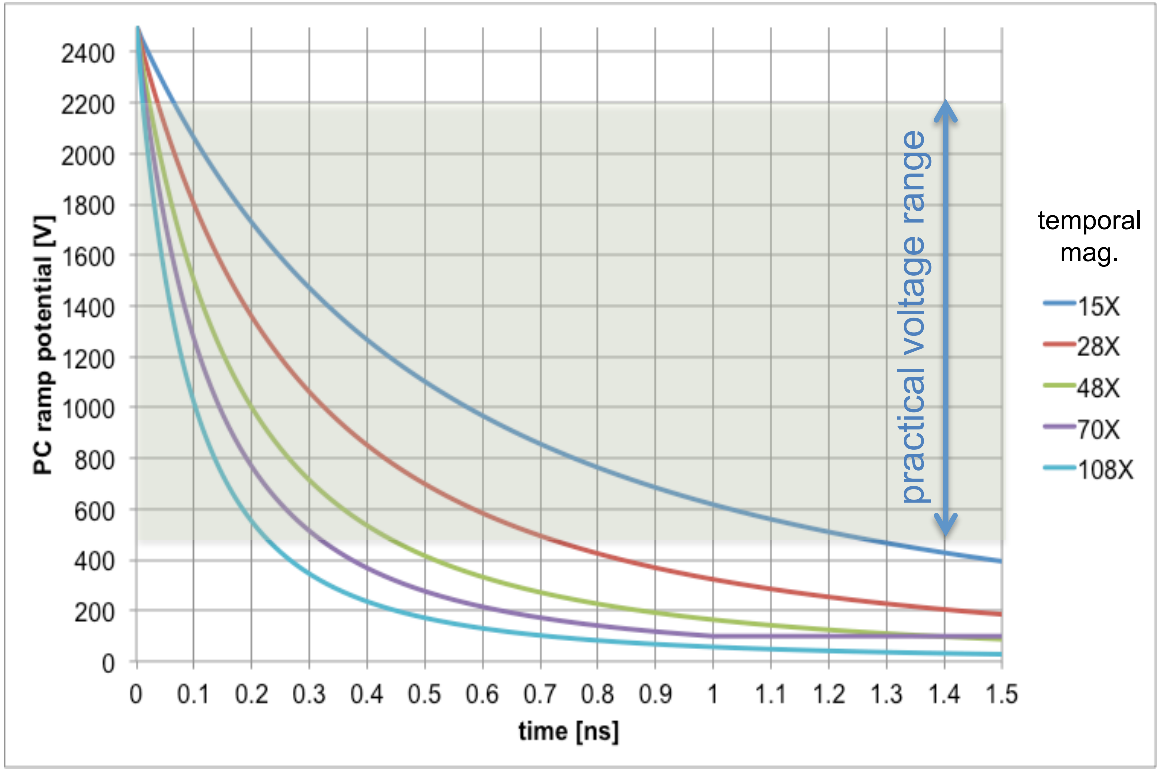
practical drift voltage range 2.5-0.5 kV

390 mm = maximum drift length we could squeeze into airbox with pulsers & camera

Photocathode ramp pulse shapes control the temporal magnificatin and recording interval

Temporal mag. depends on drift time and PC ramp rate

As potential (drift time) drops ramp rate must decrease



PC voltage profiles needed to achieve uniform temporal magnification of various magnitudes

operating modes for single strip SLOS in DIM

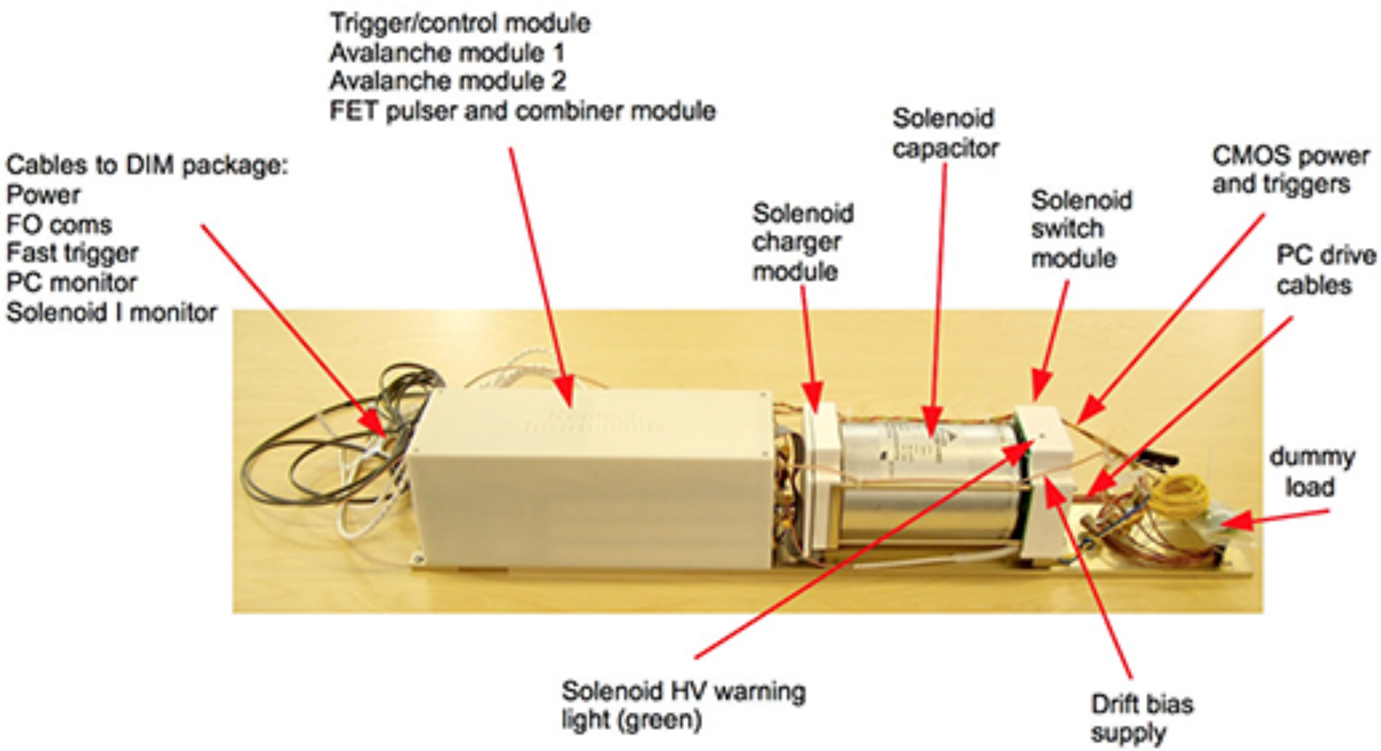
record length	gate width
190 ps	19 ps
265 ps	28 ps
390 ps	42 ps
600 ps	71 ps
1050 ps	133 ps

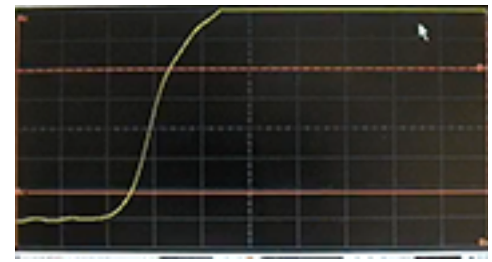
assumes 2 ns back-end gate

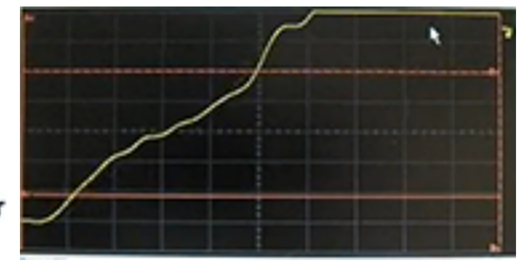
Programmable photocathode pulser allows gate width/record length to be changed on the fly

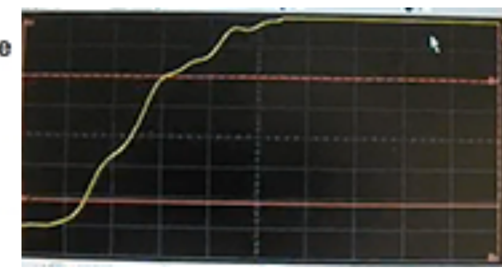
Fast ramp pulser is comprised of 8 avalanche step generators which are added together to create main pulse

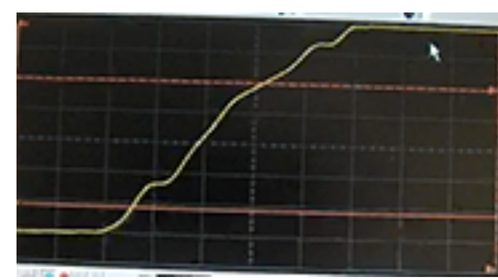
Each step generator can be independently timed via programmable delays thereby controlling ramp shape



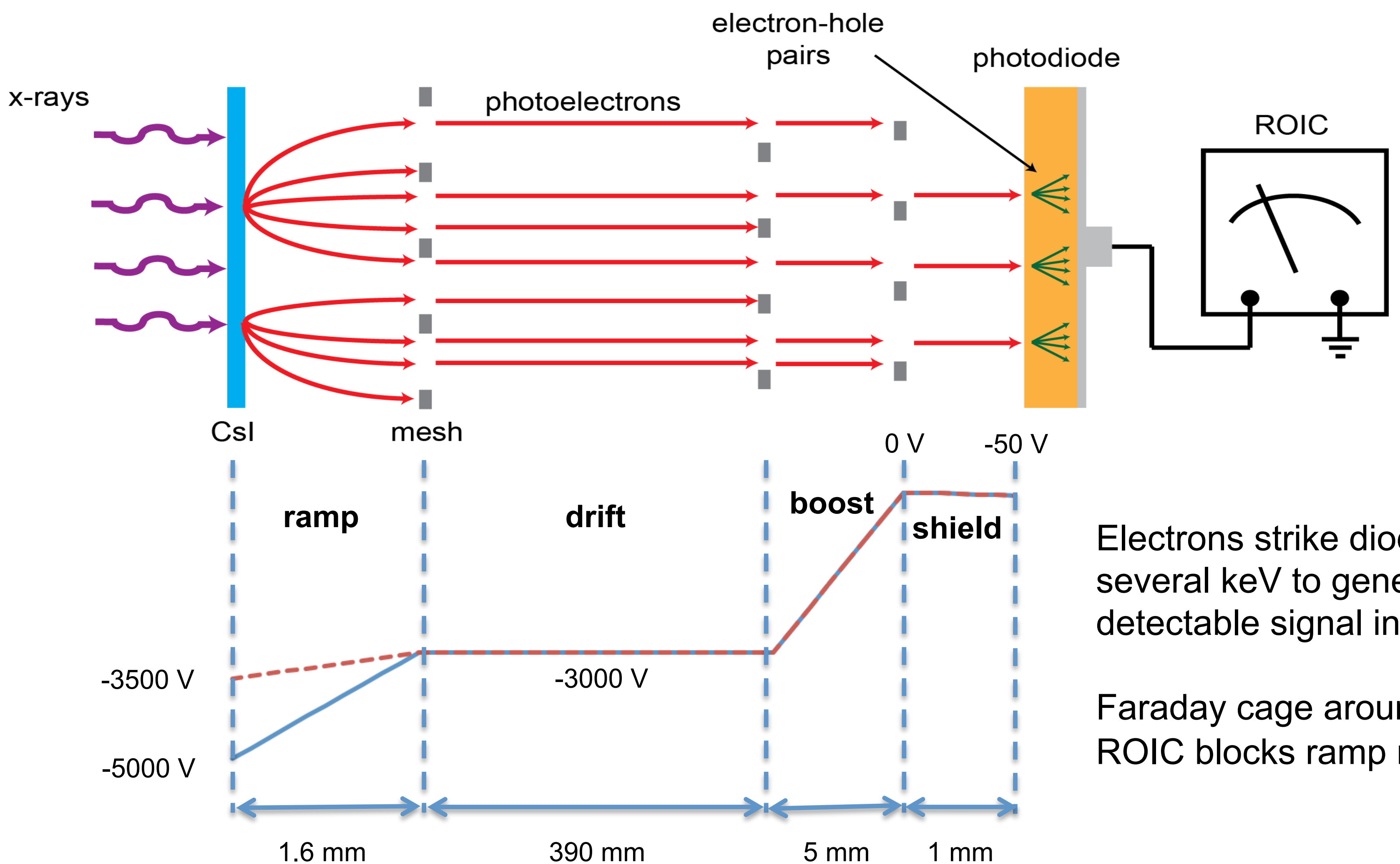








Photoelectrons pass through a 4 potential regions which accelerate, separate and then slam them into photodiode



Electrons strike diode with several keV to generate detectable signal in ROIC

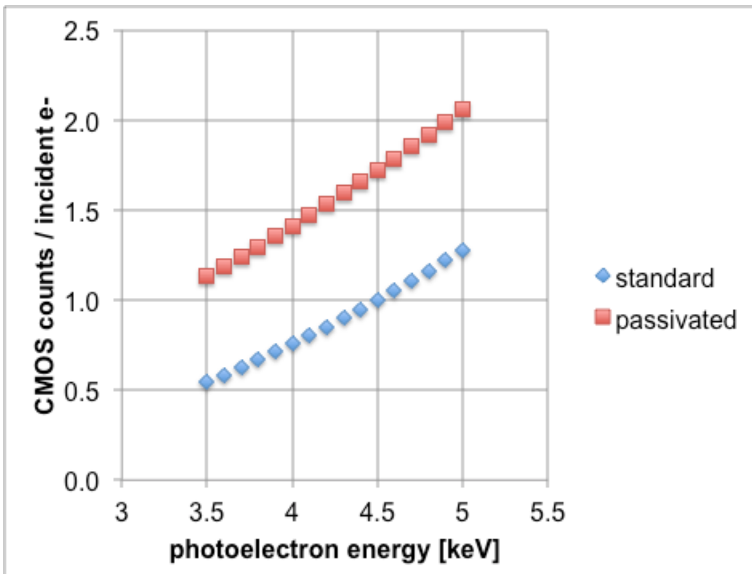
Faraday cage around ROIC blocks ramp noise

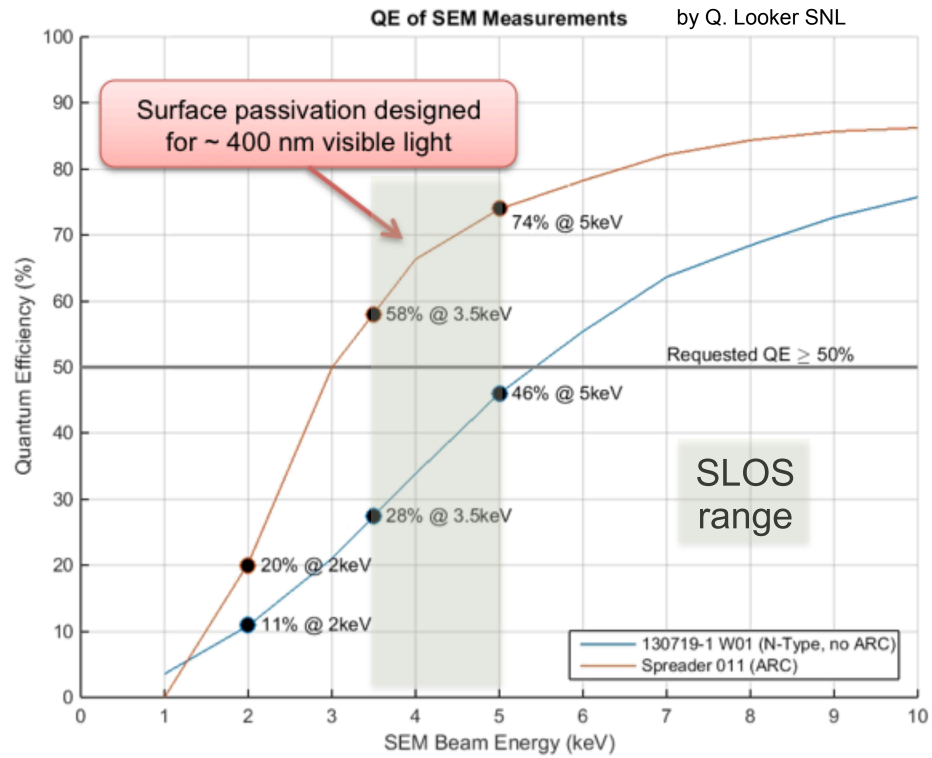
Icarus diode response to ~4keV electrons yields approximately 1 "count" per incident electron

$$\frac{N_{counts}^{CMOS}}{N_{pe}} = \frac{E_{pe} QE(E_{pe})}{E_{e-h} N_{e-h}^{\min}}$$

$E_{e-h} = 3.6\ eV$ energy to create electron hole pair

$N_{e-h}^{\min} = 500$ electron hole pair detection level



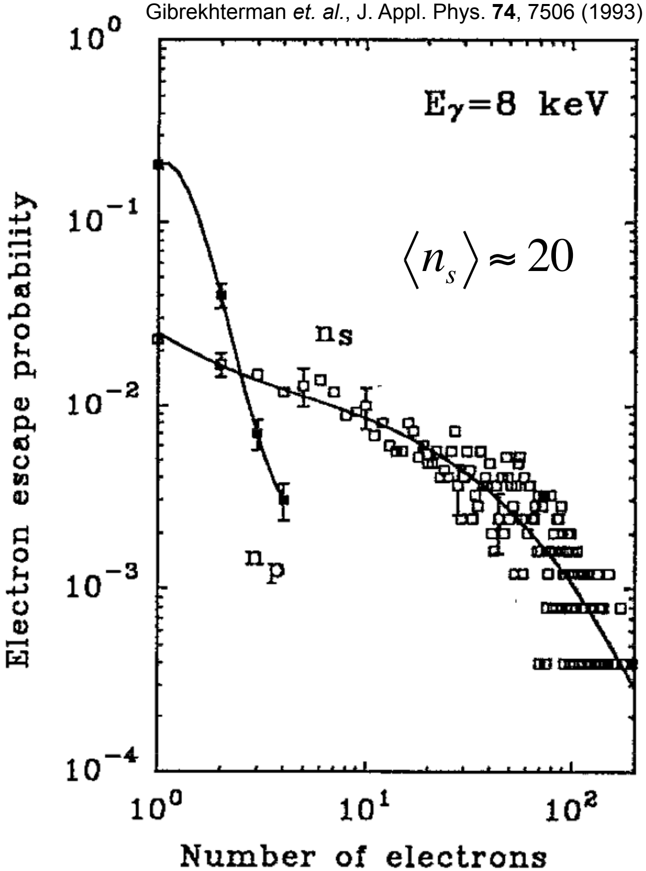


photodiode electron responsitivity about right for SLOS

some fine tuning required depending on application

Statistics of CsI photoemission dictate weak dependence of detection efficiency on photodiode responsivity to electrons

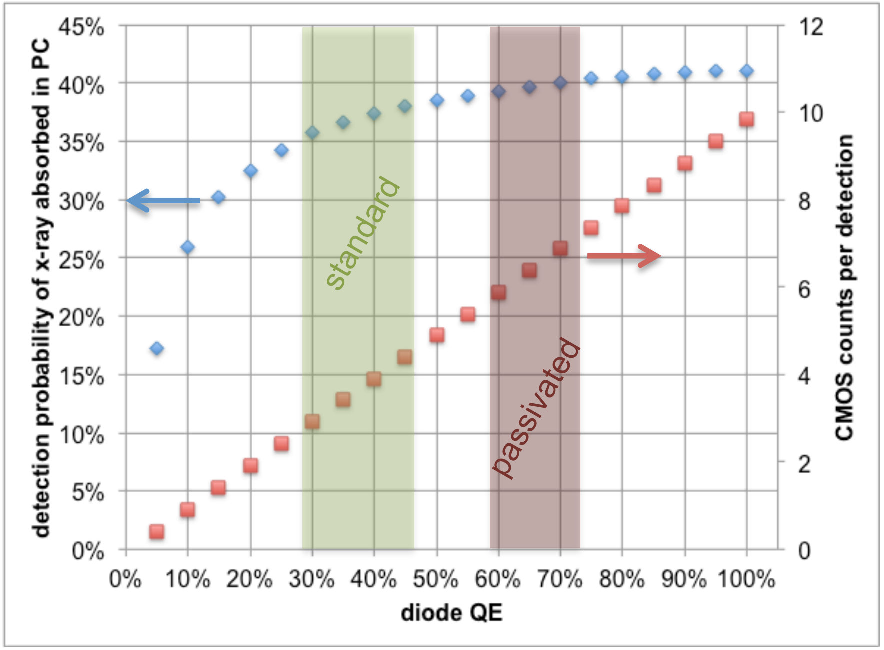
Gibrekhterman *et. al.*, J. Appl. Phys. **74**, 7506 (1993)



CsI cathode yields ~20 e$^-$ / absorbed x-ray

diode QE mainly affects dynamic range

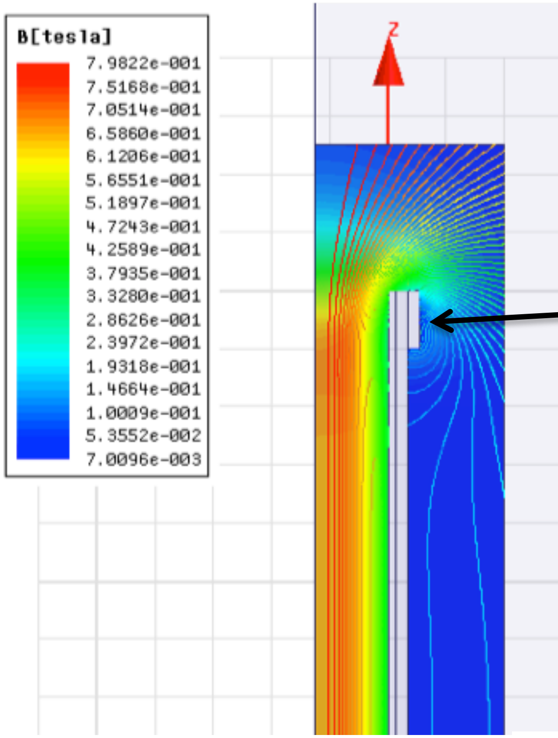
optimum QE depends on background noise
gain set by e$^-$ boost, diode QE, ROIC specs



200 nm CsI transmission photocathode

Monte Carlo simulation of 1st principles model of electron interaction with matter

Pulsed magnetic produces uniform 6 kG field for 1:1 electron imaging resulting in 40 mm spatial resolution



1 kJ for magnetic field is stored in a 295 uF 2 kV electrolytic capacitor located in the DIM

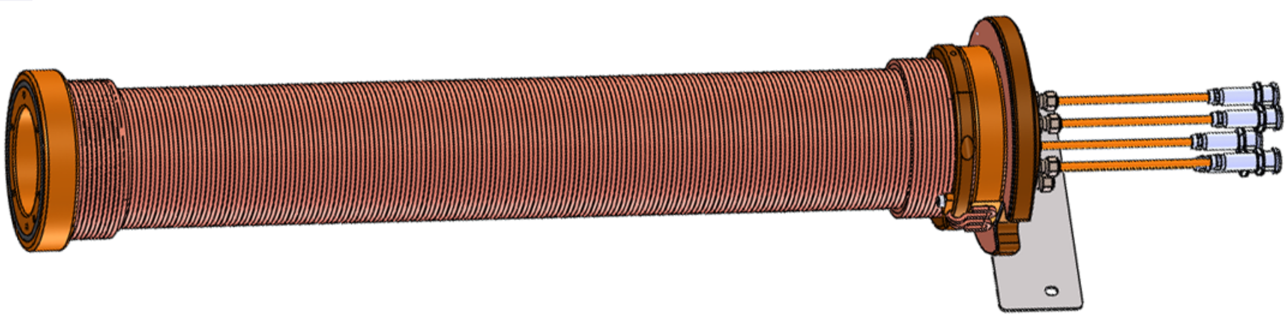
Coil wound onto vessel with a single winding

Turns doubled near the end for field shaping

$$\delta = \sqrt{(4r_L)^2 + \delta_{CMOS}^2} = 39\ \mu m\ @\ 6\ kG$$

328 x 656 pixels in 12.8 mm x 25.6 mm active area

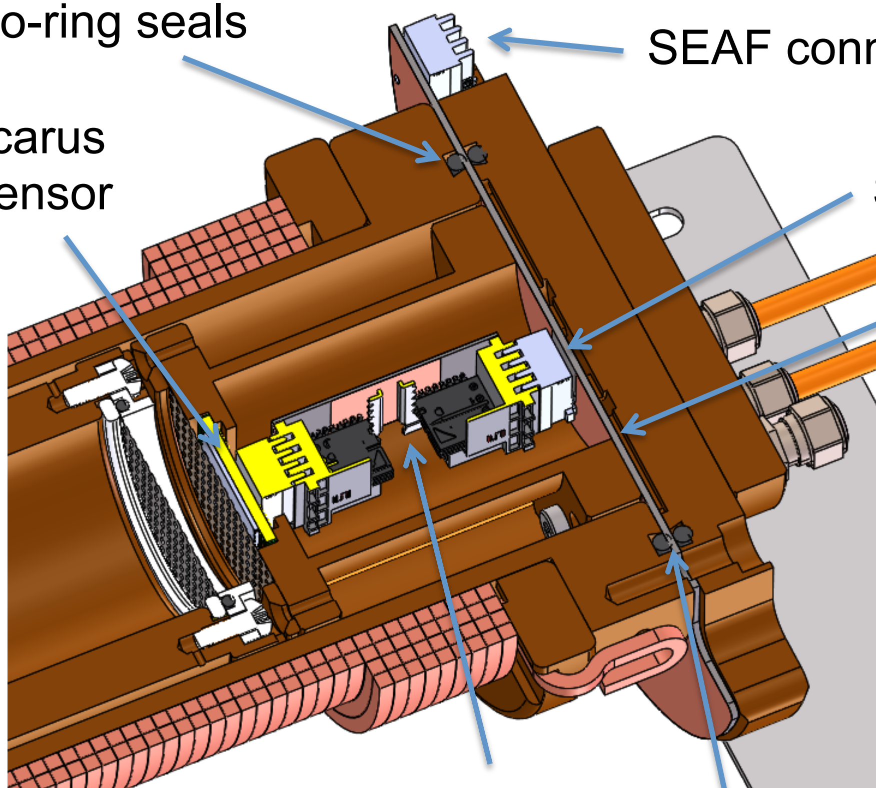
single solenoid pulser design precludes “zooming” electron image

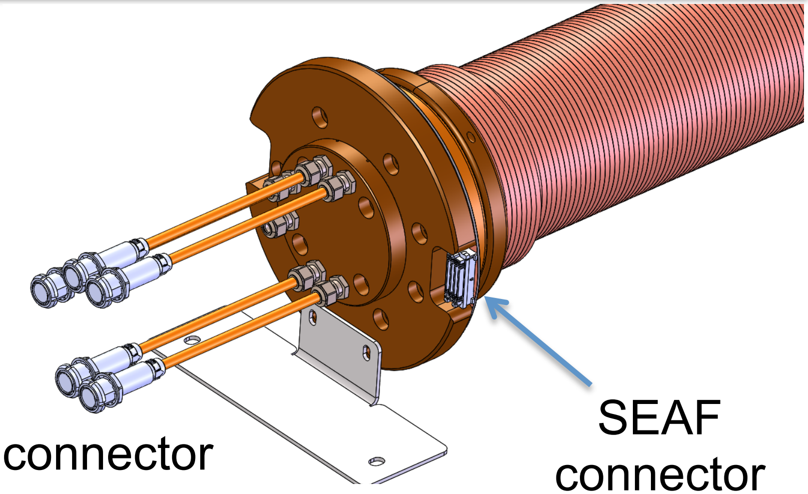


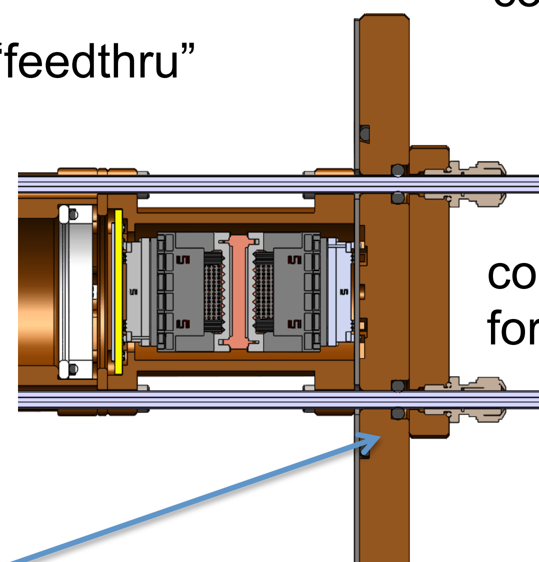
Vacuum feedthrus for Icarus sensor and HV pulsers challenging with space constraints in DIM

Icarus sensor must be locatd in vacuum

160 pins connect ROIC and camera board



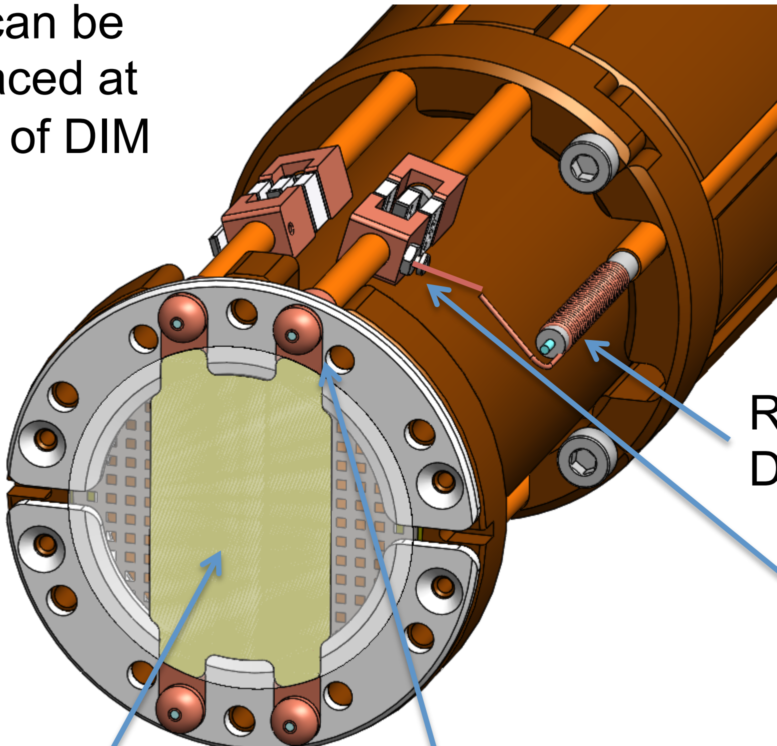




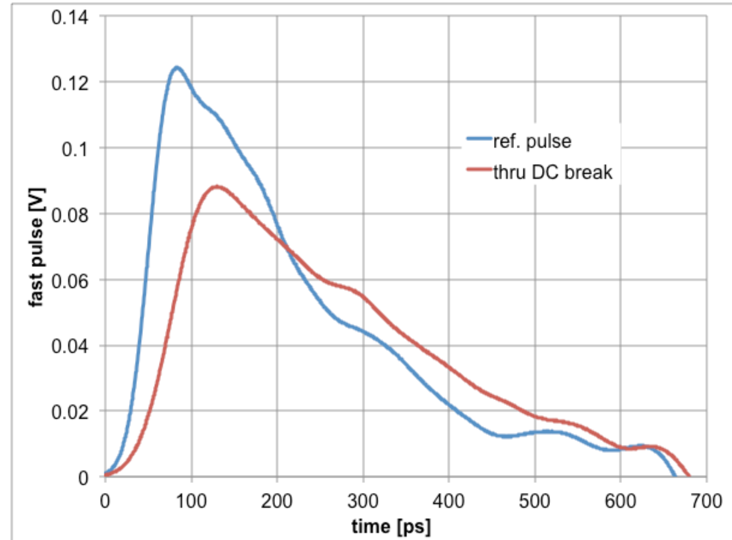
using coax & multilayer PCB as a vacuum barrier – proof tests planned

DC capacitor breaks isolate photocathode and anode cage

PC can be replaced at front of DIM

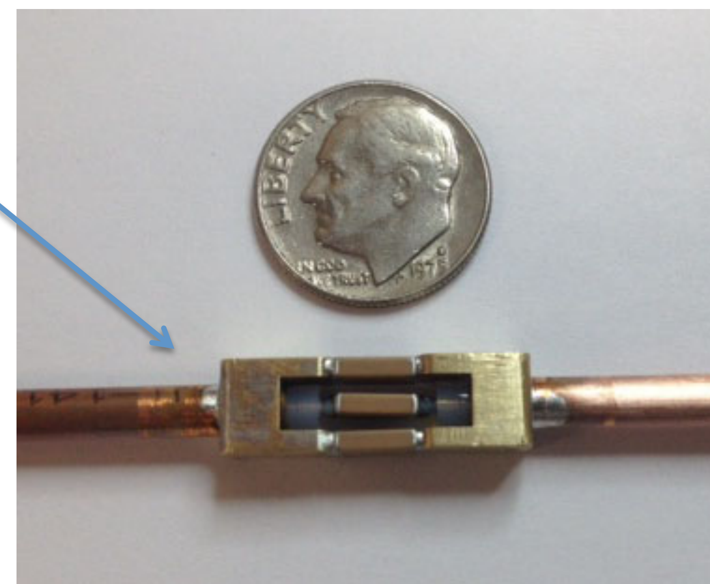


RF choke DC bias



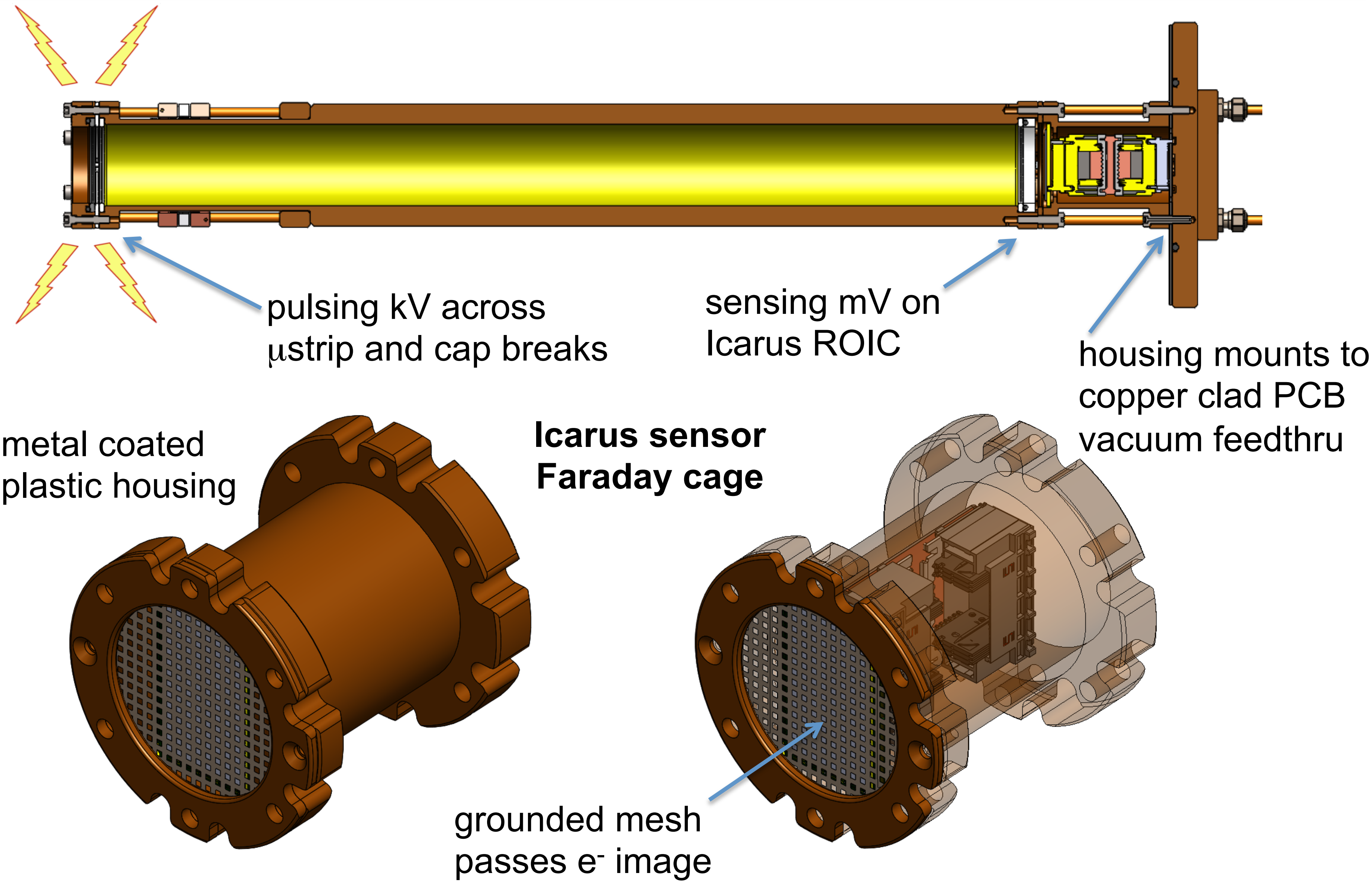
19mm wide 25 Ω PC driven by 4 coax lines

symmetric drive for colliding pulses



DC break required for coax pin and shield in order to float up anode cage for e⁻ boost

Icarus sensor must be shielded from RF noise generated by photocathode ramp at opposite end of drift tube



SLOS 1 scheduled to be taking data by end of FY16