Exceptional service in the national interest

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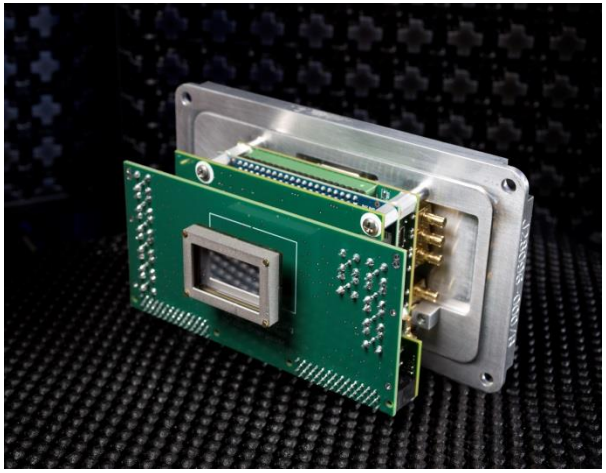

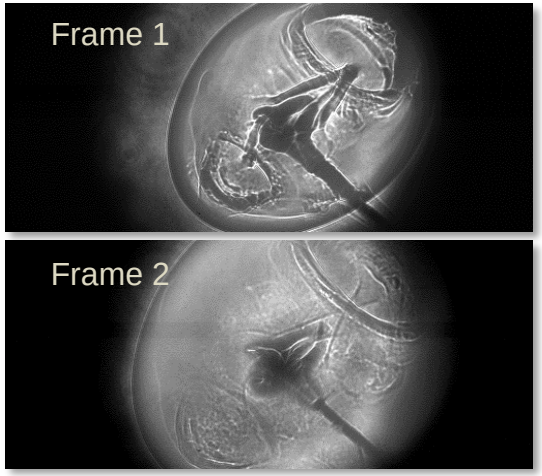

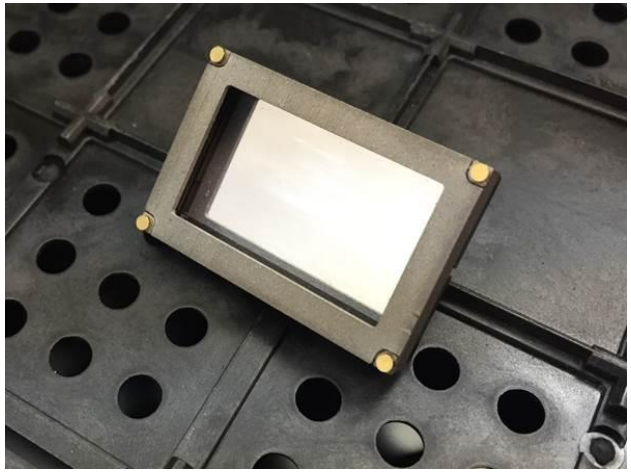

The Ultrafast X-ray Imager (UXI) Program

June 29, 2016

Liam Claus, Lu Fang, Gideon Robertson, Marcos Sanchez, John Porter, Greg Rochau

Mixed Signal ASIC/SoC Products

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U.S. DEPARTMENT OF ENERGY | NNSA National Nuclear Security Administration

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A fast, time-gated, multi-frame, hCMOS camera can offer significant benefits to HEDP diagnostics

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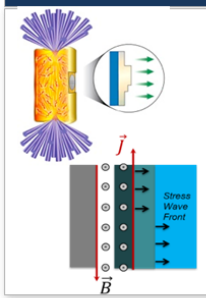
- hCMOS imagers can achieve ns level time-gating via electronic shutters
  - Multiple image frames deliver temporal history of experiments
  - Can yield improved SNR by gating out background radiation
  - CMOS scalability provides large detector area and high spatial resolution

High Pressure Materials



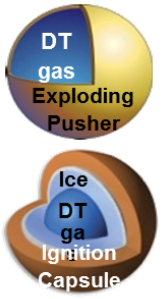
- Phase and structure
- Strength
- Conductivity
- Temperature

Complex Hydrodynamics

- High convergence radiography
- 3-D plasma conditions
- Meso-scale / Multi-shock hydro instabilities
- Mix fraction

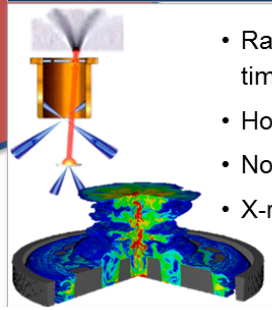
UXI FPA Capabilities

Ignition Applications and Burn



- Electron, ion temperature equilibration
- Ionization state
- Stopping power of alphas
- Radiochemistry
- Radiography/Imaging
- Burn history

Radiation Transport, Opacity, & Effects



- Radiation T, ne in 3D spatial, time
- Hohlraum conditions
- Non-thermal electrons
- X-ray source characterization

A fast, multi-frame imager offers significant potential in HEDP physics research

The UXI program has developed or has experience in the 3 key technologies required for an hCMOS imager

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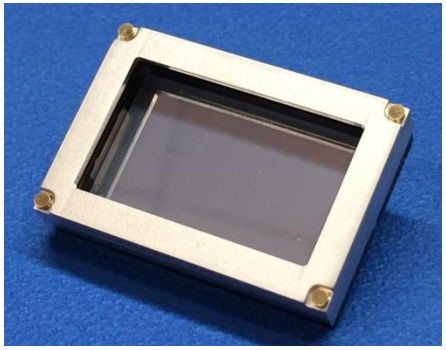
Read-Out Integrated Circuit (ROIC)

Under the UXI program, SNL has developed a portfolio of ROICs demonstrating incremental improvements and features

- 25 µm spatial resolution
- 448-512 x 1024 format
- ~ 2 ns integration time
- 2-4 frames native, 8 frames interlaced
- 500 k - 1.5 M e^- full well



Hippogriff in SOP package w/ 25 µm Si photodiodes

Detectors

Under the UXI program, SNL has developed a number of silicon detector variants:

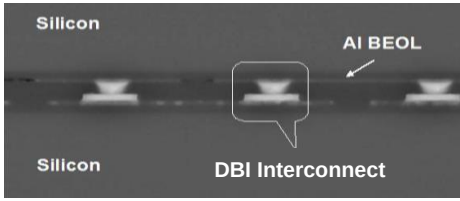
- **25 µm thick** –Vehicle for 4.7-6.1 keV X-ray, energetic electron, and visible light detectors
- **100 µm** thick – Possibly useful for up to 13 keV X-ray detection (Absorption 30% @ 13 keV)

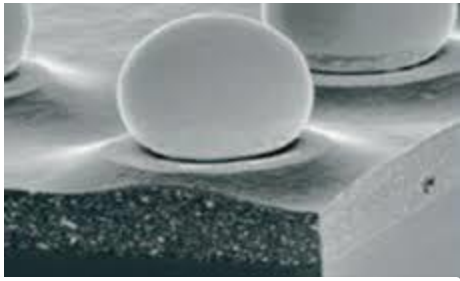
Hybridization

Indium and Direct Bond Interface (DBI) are both options:

- DBI is licensed by SNL and in development in-house
- DBI off-site at Novati
- Indium available in house

Oxide-to-oxide "Direct Bond Interface"





Indium Bump

Mixed Signal ASIC/SoC

A hybrid sensor enables independent optimization of the diode array & the readout electronics (ROIC).

Fast, silicon detectors were developed at SNL for 6 keV X-ray response and have show good response to visible light and energetic electrons

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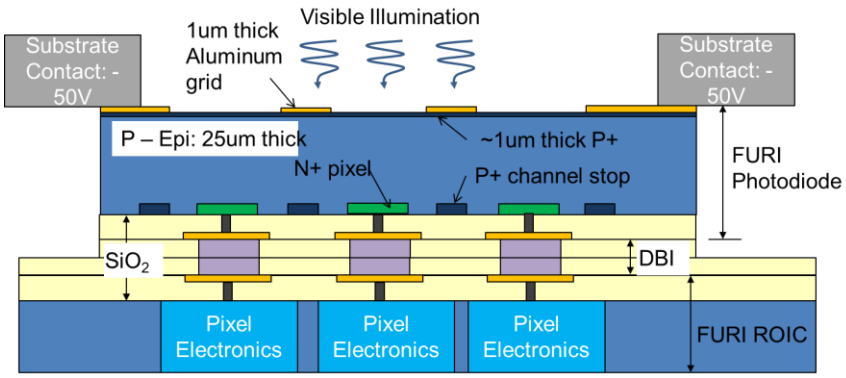
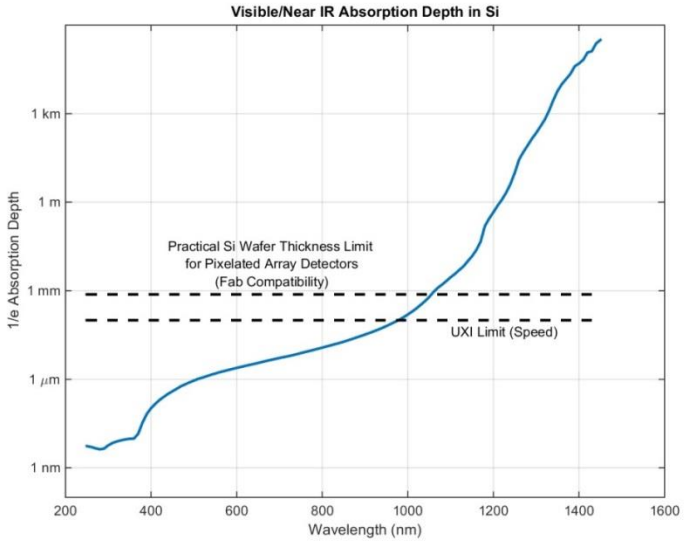
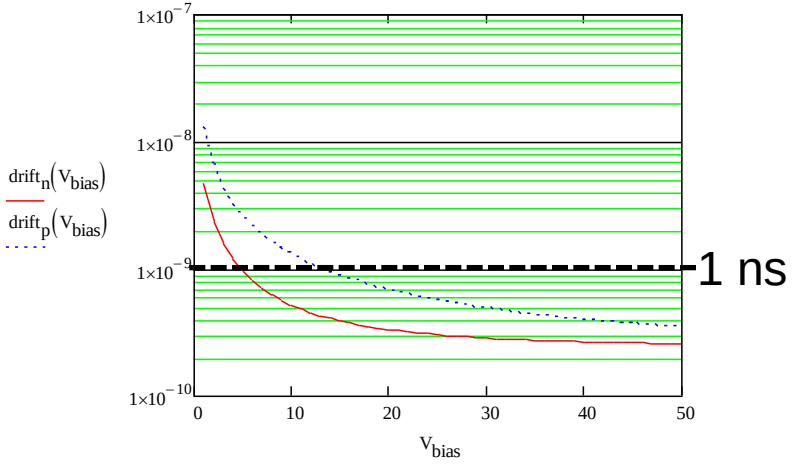
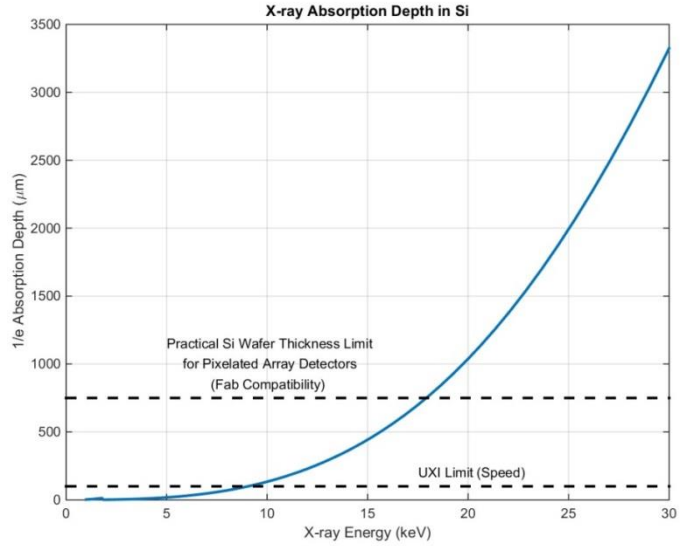




25 μm thick PD drift time vs. bias



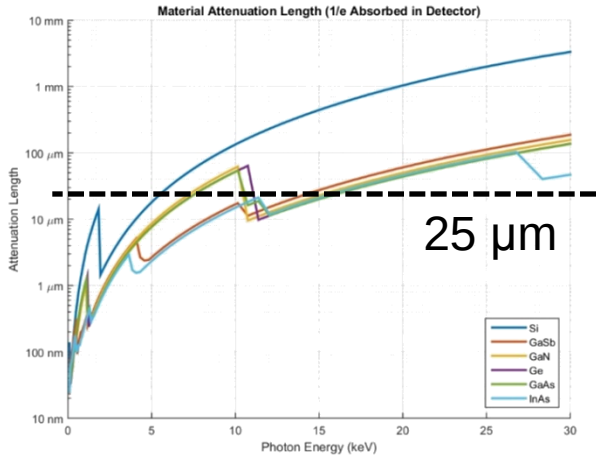


Material	Electron μ (cm^2/V-s)	Electron υ_{sat} (cm/s)	Hole μ (cm^2/V-s)	Hole υ_{sat} (cm/s)	Carrier 25 um Transit (ps)
Silicon	1400	1.0e7	450	**0.7e7**	**357**

Si photodiodes are cost effective and function well for a variety of spectra ranging from visible to low keV X-rays.

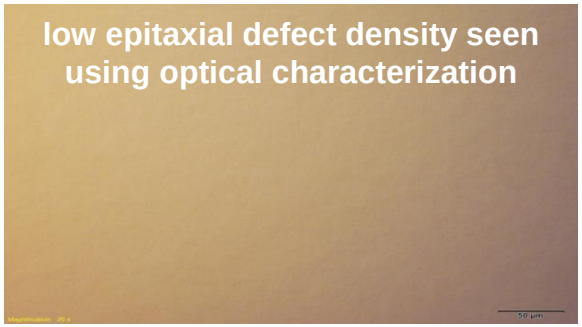
There are ongoing efforts to build III-V detectors for direct detection of higher energy X-rays

- Silicon detectors need to be thick for reasonable X-ray absorption > 10 – 15 keV, which hurts high speed performance of the detector
- III-V detectors offer an order of magnitude improvement in attenuation length

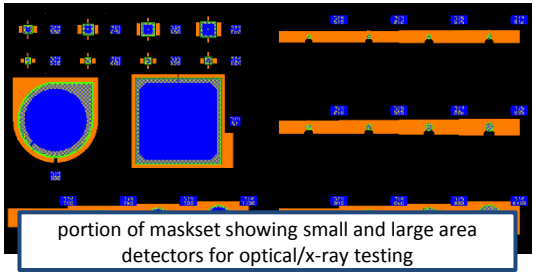


- However, significant challenges exist (discussed at CEA in 10/2015):
  - **Thick Growths** - Growing thick (> 5 µm) epi layers is unusual, process needs development for high-quality growths.
  - **Depleting Semiconductor -** Background carrier concentrations generally higher than Si, more difficult to fully deplete.
  - **Fluorescence –** Incident X-ray photons can eject fluorescence X-ray photons with relatively high energy (and thus, relatively long range)
  - **Thermal Noise –** Many III-V (and Ge) materials have bandgaps much lower than Si and need to be cooled to mitigate thermal noise.

- **Current Efforts**
  - Very high full well ROIC concepts have been discussed
  - GaAs is the III-V detector selected as it offers the best combination of performance and maturity
  - Late 2015 and 2016, 2 µm epi material was grown in our MBE chamber to assess material quality:



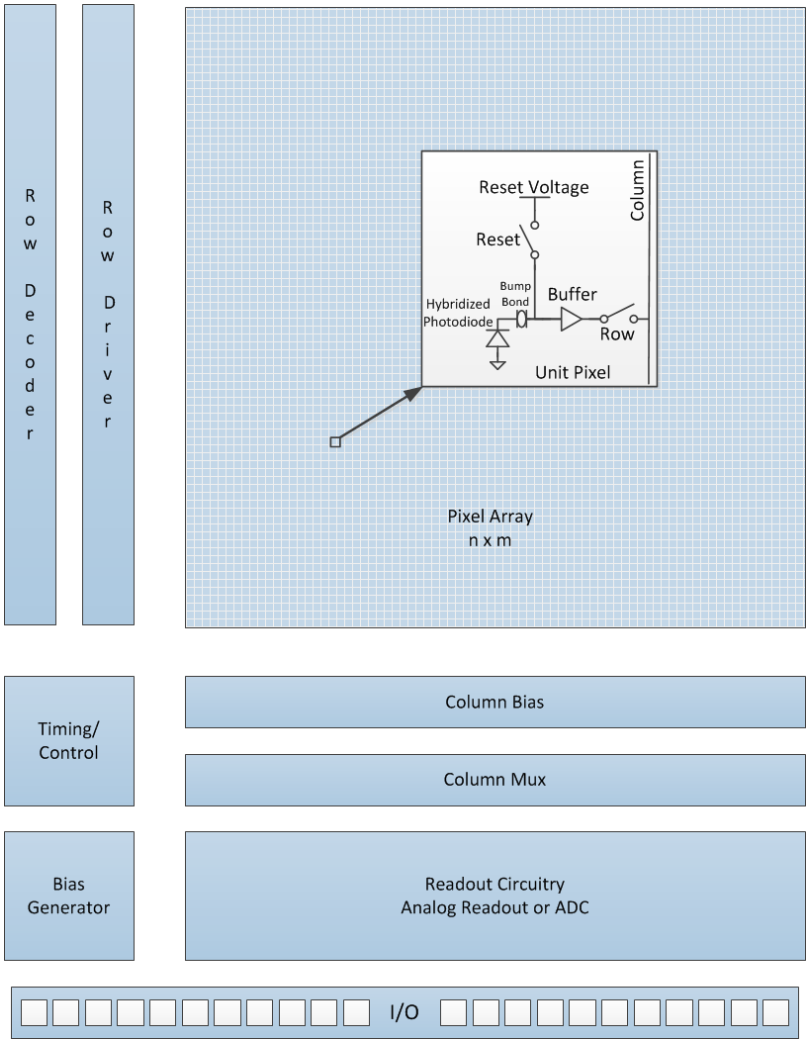
  - 20 µm material has been grown and is currently undergoing similar material quality assessments
  - 2 µm and 20 µm epi material will be patterned into discrete devices for testing in late 2016
  - GaAs diode arrays available for hybridization to UXI ROICs mid-2017



portion of maskset showing small and large area detectors for optical/x-ray testing

Traditional CMOS camera architecture serves as the starting point for fast framing cameras

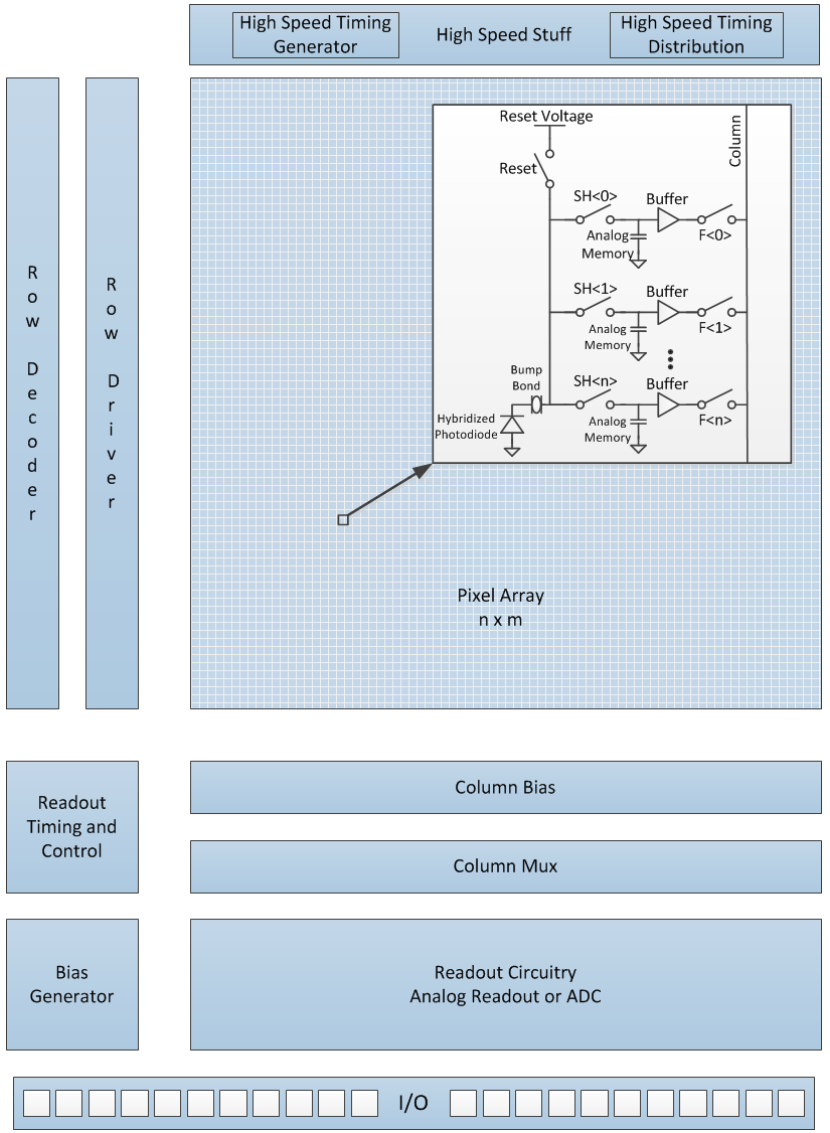
- Photodiode acts as the photon-to-electron transducer
- Pixel circuitry converts charge (Q) to a voltage or current
- Support circuitry facilitates decode and readout of the pixel array



Mixed Signal ASIC/SoC

A framing camera adds in-pixel storage to deliver multiple "frames" of data

- Multiplexes multiple pixels into one
- Transistor switch acts as an electronic "shutter"
- In pixel storage holds image data during fast sampling operation
- High speed shutters require on-chip timing generation
- Custom circuitry distributes these electronic shutters to the pixels



UXI has developed a suite of camera designs that are at various stages of development

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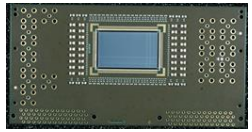
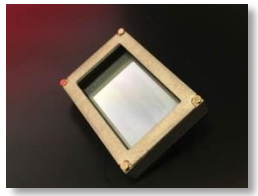
	'High' Full Well Sensors			'Low' Full Well Sensors	
	In Use		New Design	In Testing	
	Furi	**Hippogriff**	**Daedalus**	**Icarus**	**Acca (test chip)**
Year	FY14	FY15	FY17	FY16	FY18
Min. Gate	~1.5 ns	~2 ns	~1.0 ns	~1.5 ns	~1 ns
Frames	2	2 (full resolution) 4 or 8 (Row interlaced)	3 (full resolution) 6+ (Row interlaced)	4 (full resolution) 8 (L/R interlaced)	8
Tiling Option	No	No	One Side	No	Linear Tiling
CMOS Process	350 nm (SNL)		350 nm (SNL)	350 nm (SNL)	130 nm (G.F.)
Pixels	448 x 1024		512 x 1024	512 x 1024	512 x 512
Pixel Size	25 μm x 25 μm		25 μm x 25 μm	25 μm x 25 μm	
Capacitor Full Well	1.5 million e^-		1.5 million e^-	0.5 million e^-	





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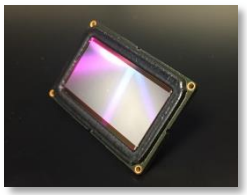

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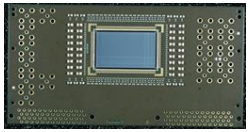
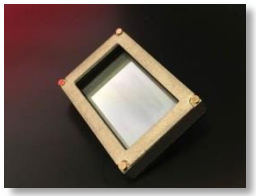
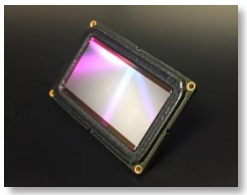




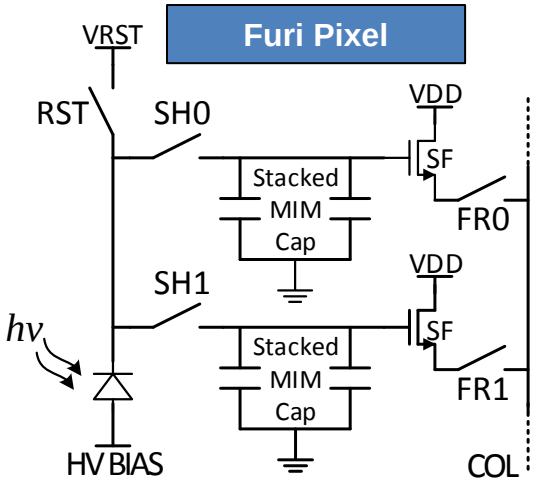
TBD

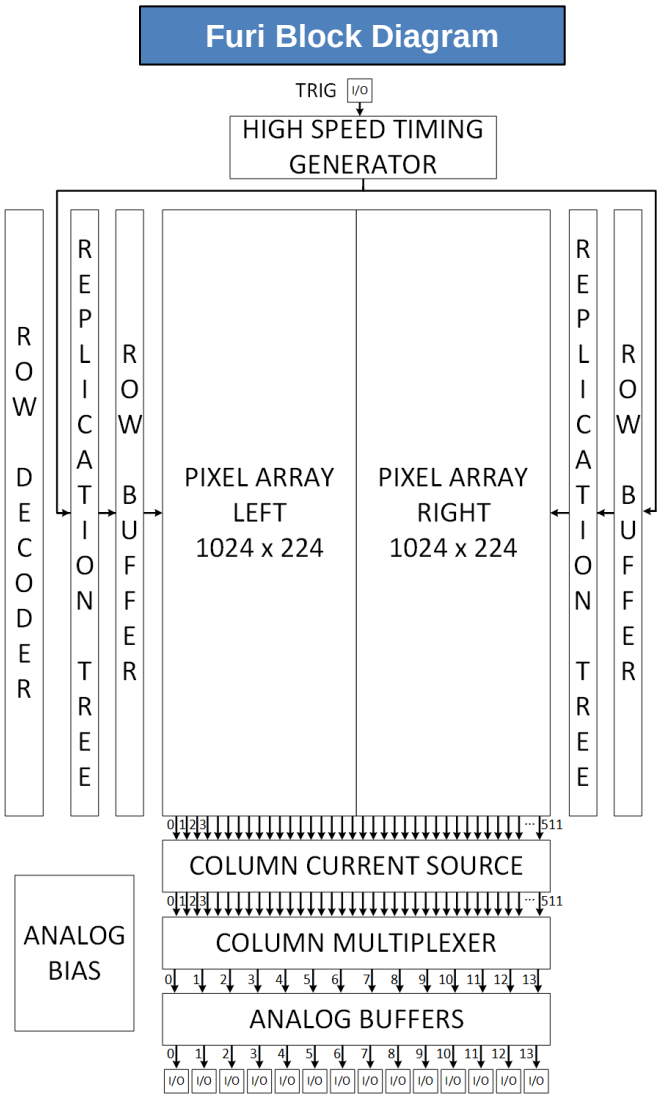


Mixed Signal ASIC/SoC

Furi was the first large scale 2-D ROIC fabricated in SNL's CMOS7 process

- ROIC features
  - 1024 x 448 pixels on 25 µm pitch
  - 2 frames
  - < 2 ns integration time
  - < 2 ns inter-frame time
  - 60 dB dynamic range
  - 1.5 M e^- full well
  - 1500 e^- noise floor
  - Common anode detector
  - Asynchronous triggered, low jitter, fast startup oscillator
  - Programmable timing pattern generator
  - Timing driven to L/R hemispheres to reduce row RC





Active array size: 11.2 mm x 25.6 mm

Mixed Signal ASIC/SoC

Furi's primary goal was to investigate high speed timing generation and propagation across a large die

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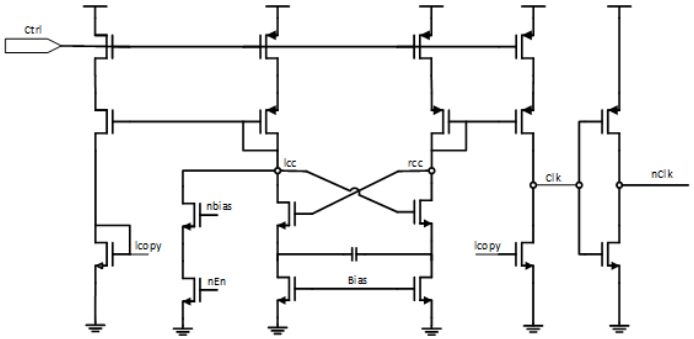
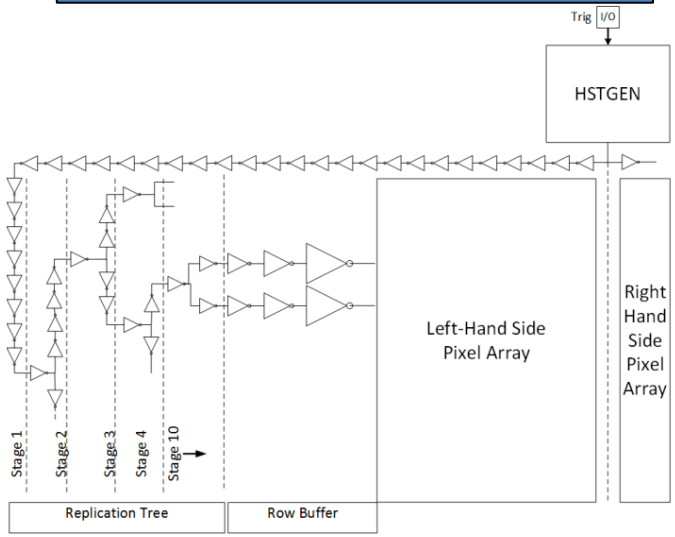
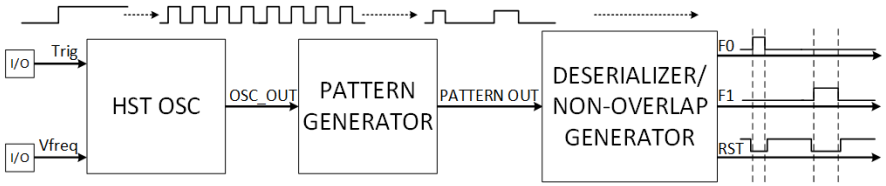
Fast Startup Oscillator



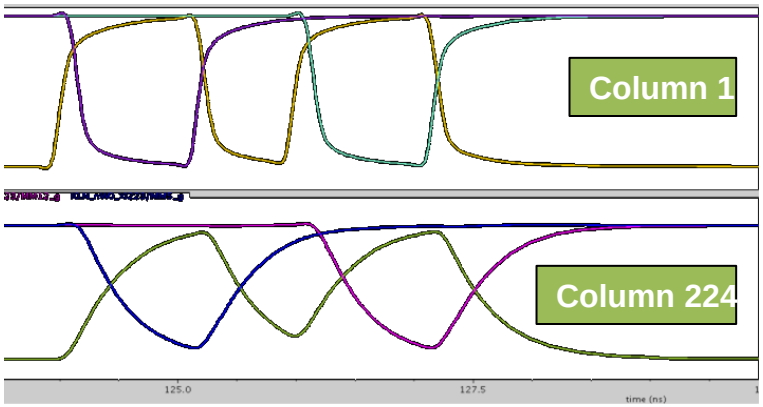
Timing Distribution



Adjustable Timing Generator



Row Shutter Signal Degradation

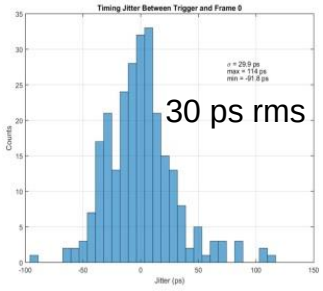


Mixed Signal ASIC/SoC

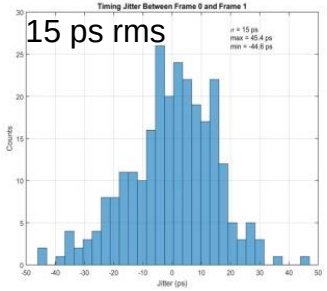
Furi was fully functional and delivered significant learning to the design team

- ROIC accomplishments
  - Fabrication started in September 2012
  - 48.75% yield
  - Largest die fabricated in CMOS7 at SNL
  - All design blocks were fully functional
  - Good image performance to 2 ns T_{int}
  - Currently used by Z-Machine and NIF
- Room for improvement
  - Improve shutter quality at 2 ns
  - Improve minimum shutter speed < 2 ns T_{int}
  - L/R hemisphere timing errors
    - Close to 900 ps
  - 33% L/R hemisphere gain error
  - Frame-to-frame coupling ~10%
  - 50 % F-F gain error at larger input signals
    - IR drop (replacement current)

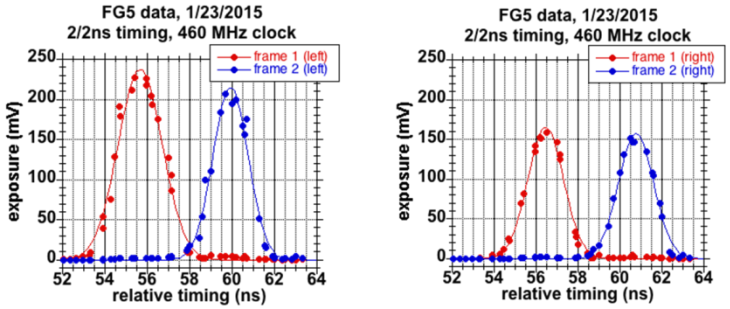
Trigger-To-Shutter Jitter



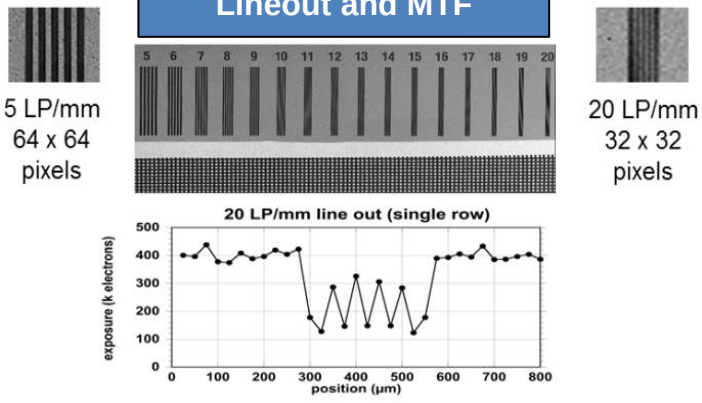
Shutter-To-Shutter Jitter



2 ns Gate Profiles



Lineout and MTF



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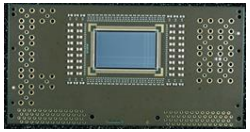
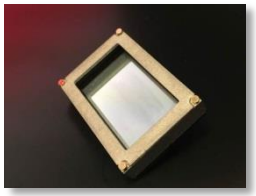
Pixel Size	25 μm x 25 μm		25 μm x 25 μm	25 μm x 25 μm	
Capacitor Full Well	1.5 million e^-		1.5 million e^-	0.5 million e^-	





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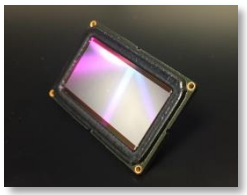
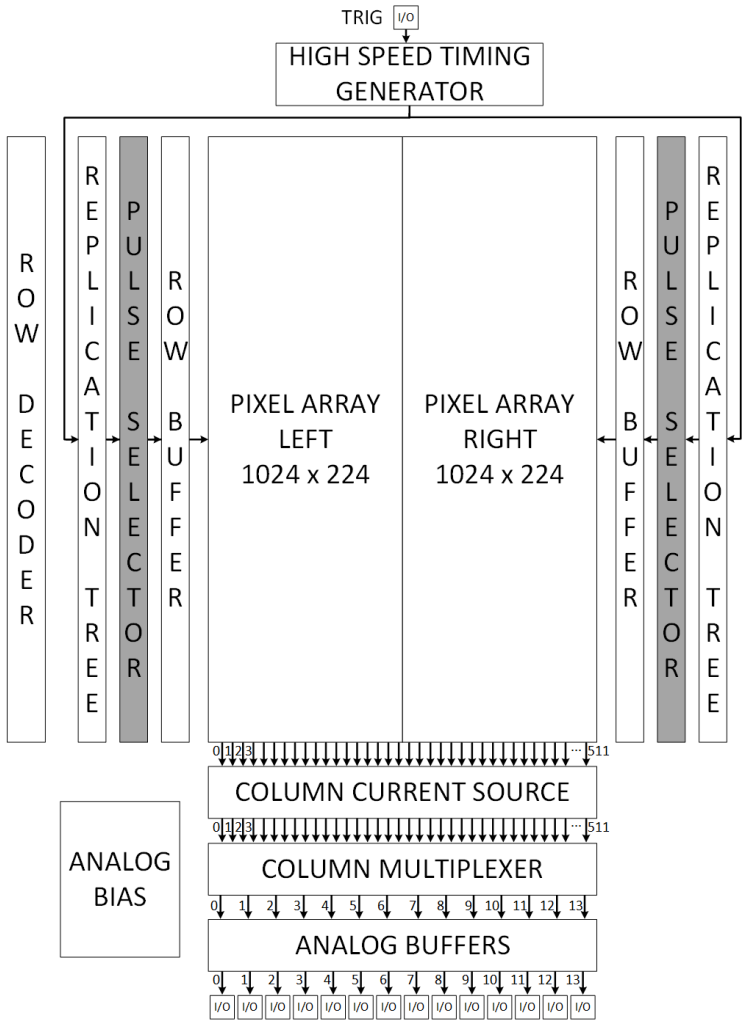


Mixed Signal ASIC/SoC

Hippogriff was a fast iteration leveraging as much Furi IP as possible while adding interlacing functionality

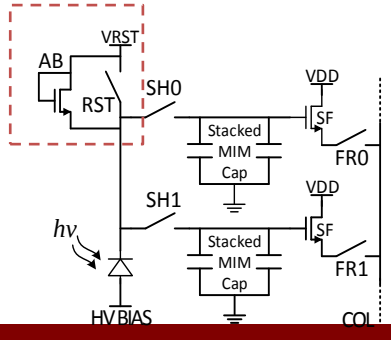
- ROIC features
  - 1024 x 448 pixels on 25 µm pitch
  - 2 frames
  - < 2 ns integration time
  - < 2ns inter-frame time
  - 60 dB dynamic range
  - 1.5 M e- full well
  - 1500 e- noise floor
  - Common anode detector
- Improvements/modifications on previous ROICs
  - Added interlacing capability to trade spatial resolution for number of frames
    - Up to 4 rows/8 frames
  - Improved predicted hemisphere timing offsets
  - Integrated anti-bloom transistor in pixel

Hippogriff Block Diagram



Active array size: 11.2 mm x 25.6 mm

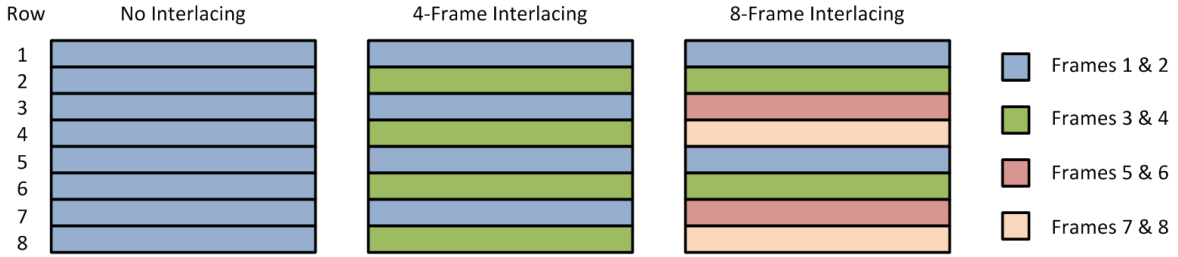
Hippogriff Pixel



Mixed Signal ASIC/SoC

Hippogriff was designed to explore adding more frames at relatively low design cost and time

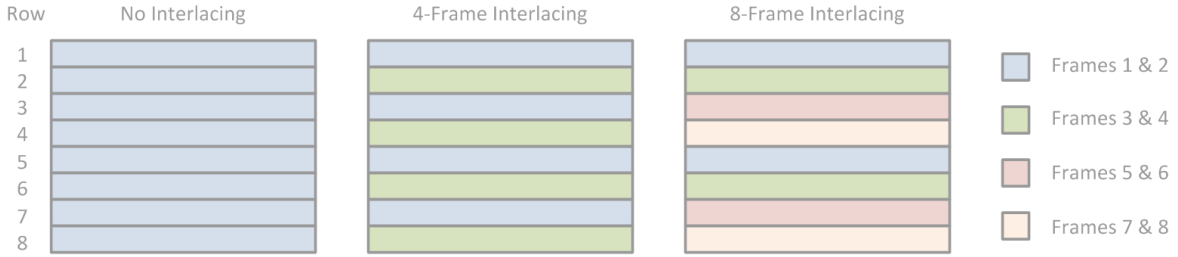
- Hippogriff Implements 2 Special Timing Modes:
  1. **Row Interlacing:** Allows a user to trade spatial resolution for additional frames



# Frames	Frame Resolution
2	1024 x 448
4	512 x 448
8	256 x 448

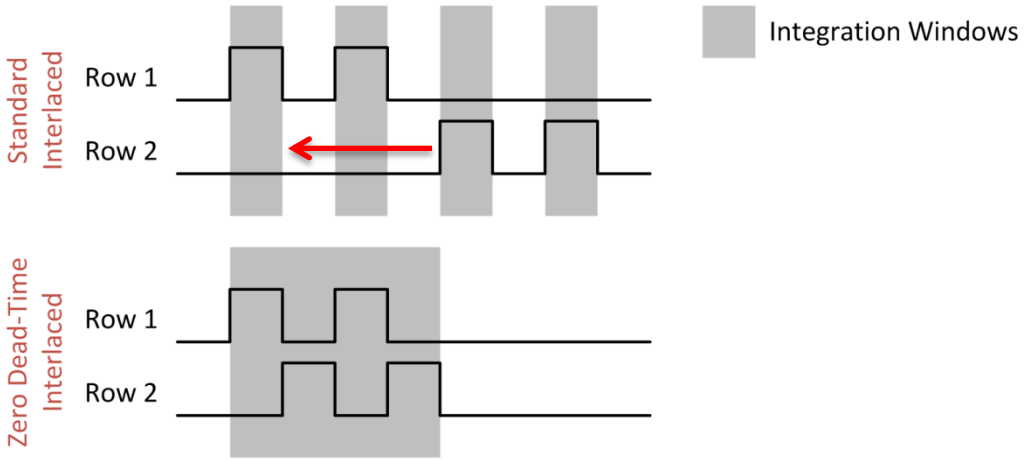
Hippogriff was designed to explore adding more frames at relatively low design cost and time

- Hippogriff Implements 2 Special Timing Modes:
  1. **Row Interlacing:** Allows a user to trade spatial resolution for additional frames.



# Frames	Frame Resolution
2	1024 x 448
4	512 x 448
8	256 x 448

  2. **Zero Dead Time ("Movie") Mode:**
     - Suitable for use only fastest T_{int} configuration
     - Provides approximately zero dead time between frames
     - Note that this is implemented with relatively crude circuits.

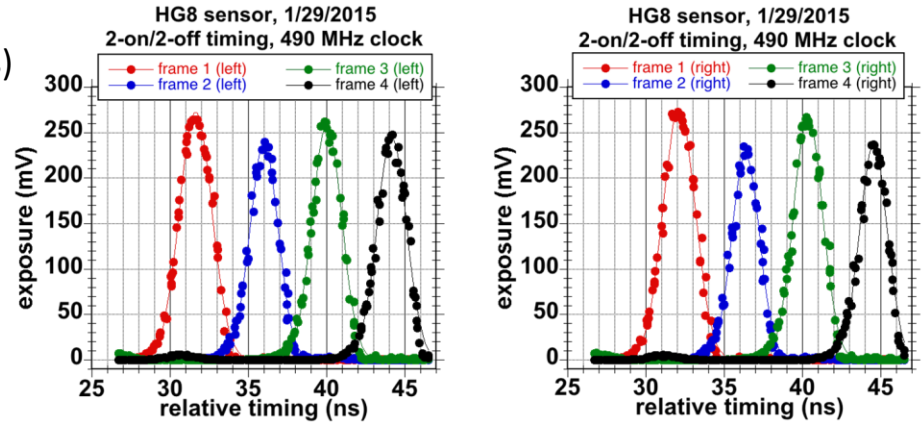


Mixed Signal ASIC/SoC

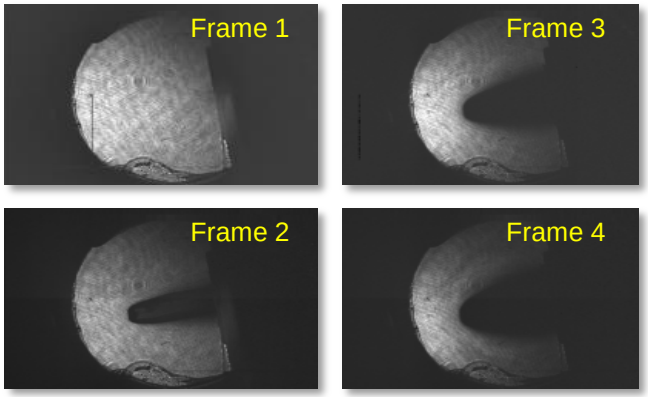
Hippogriff demonstrated that our interlacing concept worked

- ROIC accomplishments
  - Fabrication started in April 2013
  - 30.2% yield
  - Improved L/R timing errors by ~50% (200-500 ps)
  - Interlacing feature works
  - Good image performance to 2 ns T_{int}
  - Currently in use in SNL Z facility laser test chambers
- Room for improvement
  - Similar performance to Furi at 2 ns T_{int}
  - Movie mode had significant R-R and F-F variation
  - Still have L/R hemisphere timing errors (up to 500 ps)
  - Same L/R hemisphere gain errors Furi
  - Same frame-to-frame coupling as Furi

Shutter Profile of 4 Frame Mode



Sequence of 4 Images, 4 ns Timing

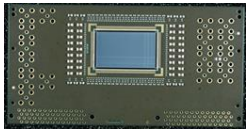


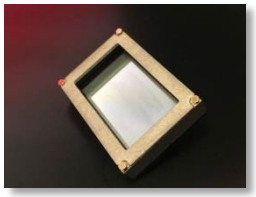
Mixed Signal ASIC/SoC

UXI has developed a suite of camera designs that are at various stages of development

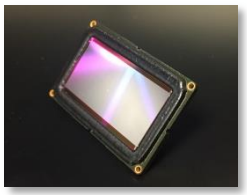
Sandia National Laboratories

	'High' Full Well Sensors			'Low' Full Well Sensors	
	In Use		New Design	In Testing	
	Furi	Hippogriff	Daedalus	Icarus	Acca (test chip)
Year	FY14	FY15	FY17	FY16	FY18
Min. Gate	~1.5 ns	~2 ns	~1.0 ns	~1.5 ns	~1 ns
Frames	2	2 (full resolution) 4 or 8 (Row interlaced)	3 (full resolution) 6+ (Row interlaced)	4 (full resolution) 8 (L/R interlaced)	8
Tiling Option	No	No	One Side	No	Linear Tiling
CMOS Process	350 nm (SNL)		350 nm (SNL)	350 nm (SNL)	130 nm (G.F.)
Pixels	448 x 1024		512 x 1024	512 x 1024	512 x 512
Pixel Size	25 µm x 25 µm		25 µm x 25 µm	25 µm x 25 µm	
Capacitor Full Well	1.5 million e^-		1.5 million e^-	0.5 million e^-	





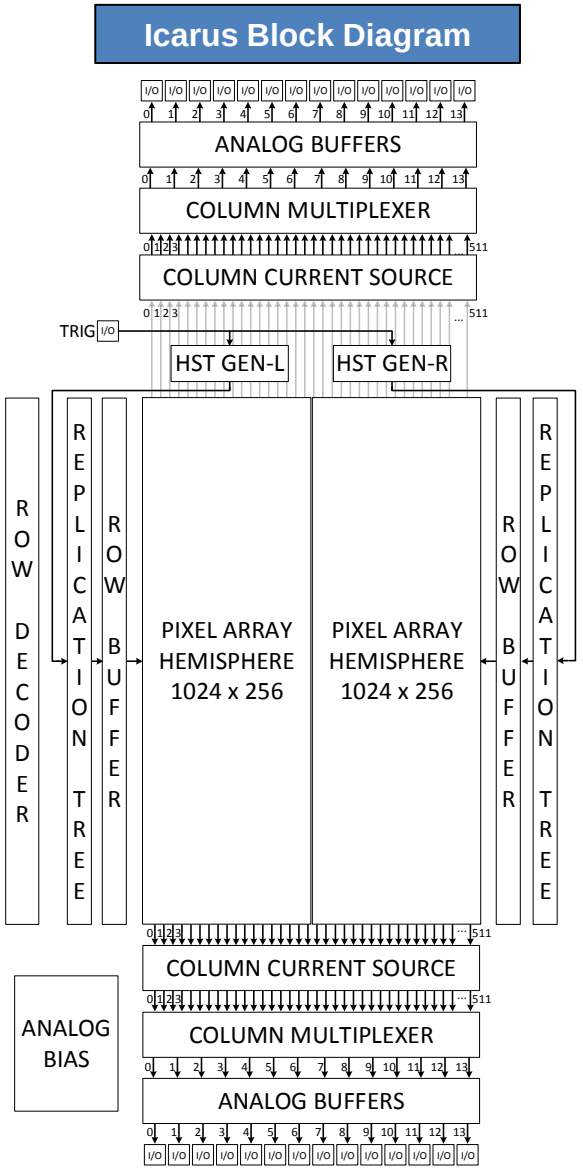
TBD



Mixed Signal ASIC/SoC

Icarus represented somewhat of a departure from the previous ROICs

- ROIC features
  - 1024 x **512** pixels on 25 um pitch
  - **4 frames**
  - < 2 ns integration time
  - < 2ns inter-frame time
  - 60 dB dynamic range
  - **500 ke$^-$ full well**
  - **500 e$^-$ noise floor**
  - **Common Cathode detector**
- Improvements/modifications on previous ROICs
  - Tunable anti-bloom transistor
  - Fully independent hemisphere timing
    - No row-wise interlacing
  - Increased HST generator pattern register depth to 40 bits
  - L/R hemisphere shutter timing tuning capability
  - Shorted intermediate reptree output stages to improve R-R timing error
  - Top/Bottom readout channels
  - CC pixel allows a more robust power distribution architecture
  - Incorporated on chip bypass capacitors



Mixed Signal ASIC/SoC

Icarus was a refinement on timing and improvement to the pixel design and power rails

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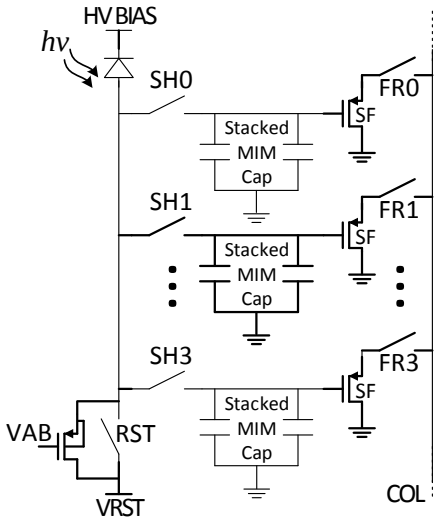
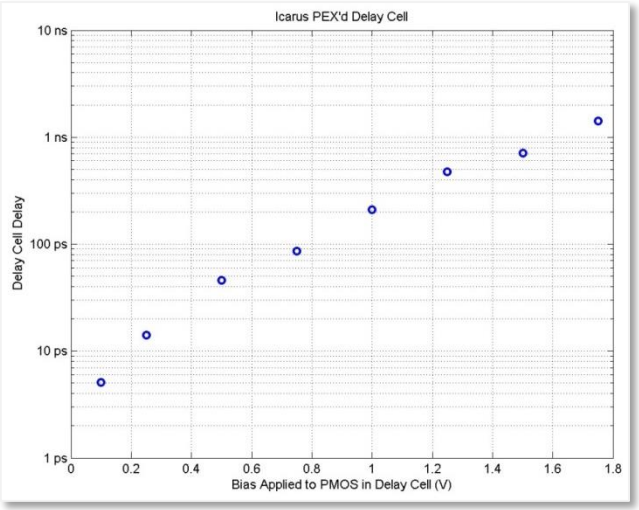
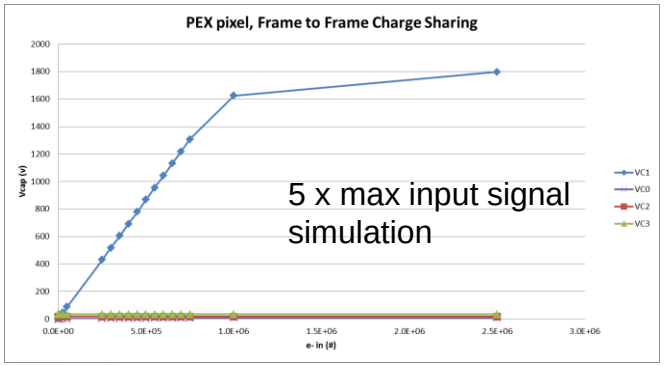
Icarus Pixel Block Diagram



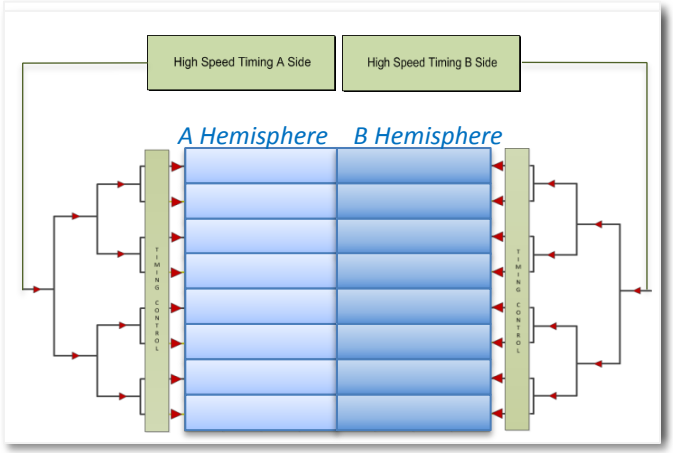
L/R Hemisphere Fine Tuning



Anti-bloom Transistor Performance Sim



Timing Distribution

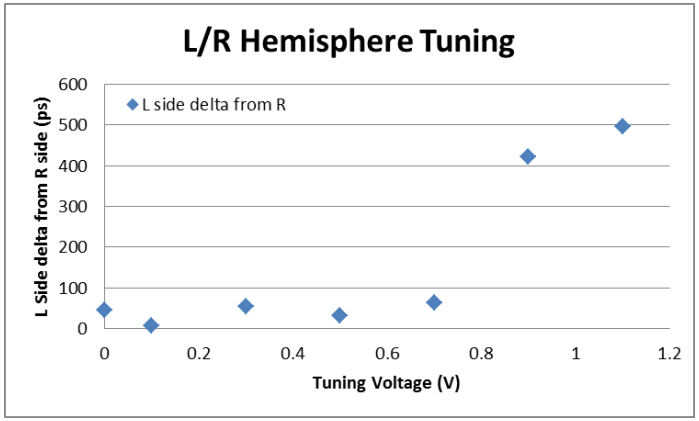


Mixed Signal ASIC/SoC

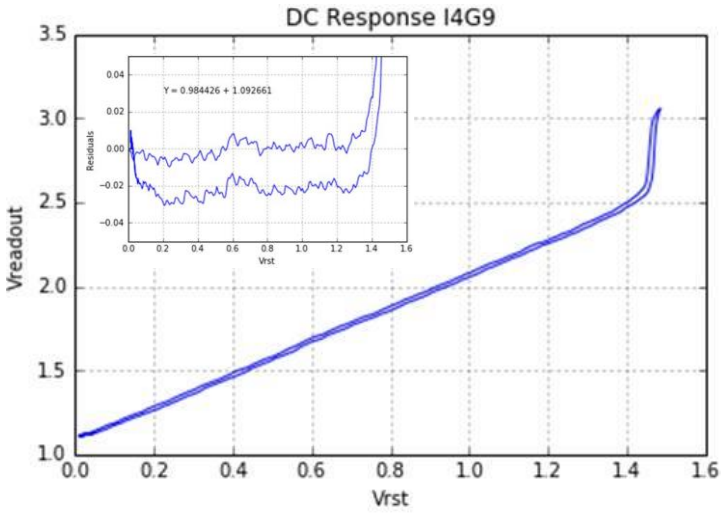
Icarus has undergone initial electrical testing and is close to first photons-on-camera characterization

- ROIC accomplishments
  - Fabrication started in April 2013
  - 45% yield
  - Independent L/R timing works
  - Native L/R timing errors improved
  - L/R tuning operates as expected so L/R timing error has been minimized
  - All timing modes work to 1:1 timing but can't build shutter profiles without photon testing
- Room for improvement
  - Need image testing to verify:
    - L/R gain errors
    - Row skew
    - Shutter profiles
    - F-F coupling
  - Photodiode design issue encountered
    - Shorted middle two columns of photodiodes to VSS
    - Short term fix
      - Etched out shorted columns from existing camera wafers
    - Redesigned photodiodes are in fab now
    - Short-term fix packaged Icarus should be delivered 07/01/16
    - Complete fix Icarus should be delivered Q1, FY17

Icarus Timing Tuning Electrical Test Results



DC Dynamic Range Sweep



Mixed Signal ASIC/SoC

UXI has developed a suite of camera designs that are at various stages of development

Sandia National Laboratories

	'High' Full Well Sensors			'Low' Full Well Sensors	
	In Use		New Design	In Testing	
	Furi	Hippogriff	Daedalus	Icarus	Acca (test chip)
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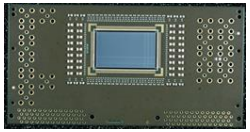
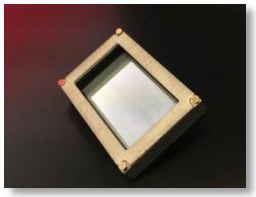
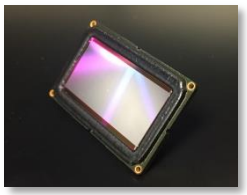
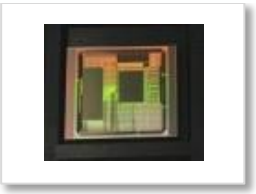
Frames	2	2 (full resolution) 4 or 8 (Row interlaced)	3 (full resolution) 6+ (Row interlaced)	4 (full resolution) 8 (L/R interlaced)	8
Tiling Option	No	No	One Side	No	Linear Tiling
CMOS Process	350 nm (SNL)		350 nm (SNL)	350 nm (SNL)	130 nm (G.F.)
Pixels	448 x 1024		512 x 1024	512 x 1024	512 x 512
Pixel Size	25 µm x 25 µm		25 µm x 25 µm	25 µm x 25 µm	
Capacitor Full Well	1.5 million e^-		1.5 million e^-	0.5 million e^-	





TBD

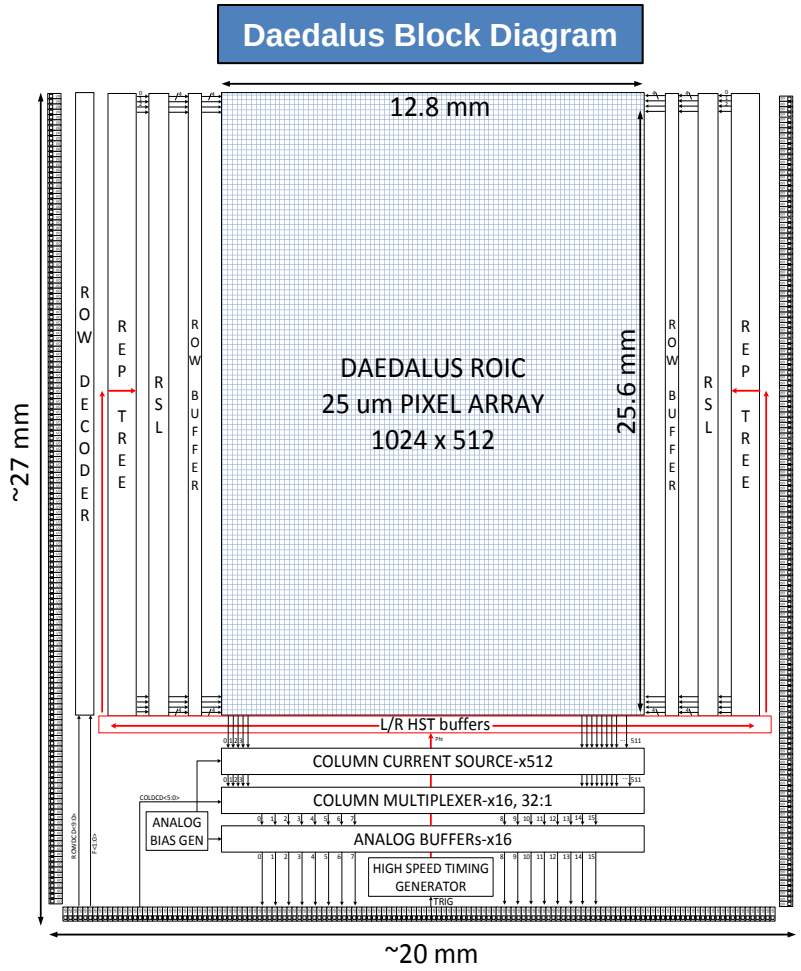




Mixed Signal ASIC/SoC

Daedalus is leveraging all the test data and learning we have obtained to date to improve on previous ROIC performance

- ROIC features
  - 1024 x 512 pixels on 25 µm pitch
  - **3 frames**
  - **< 1.5 ns integration time**
  - **< 1.5 ns inter-frame time**
  - **70 dB dynamic range**
  - 1.5 M e- full well
  - 500 e- noise floor
  - Common Cathode detector
- Improvements/modifications on previous ROICs
  - Serial encoded shutter clock distribution concept with row-wise shutter generation
  - Infinite interlacing capability
  - Improve row timing skew to <150 ps
  - 1 side abutable for a 512 x 2048 possible tiled imager
  - Test vehicle for through silicon via development

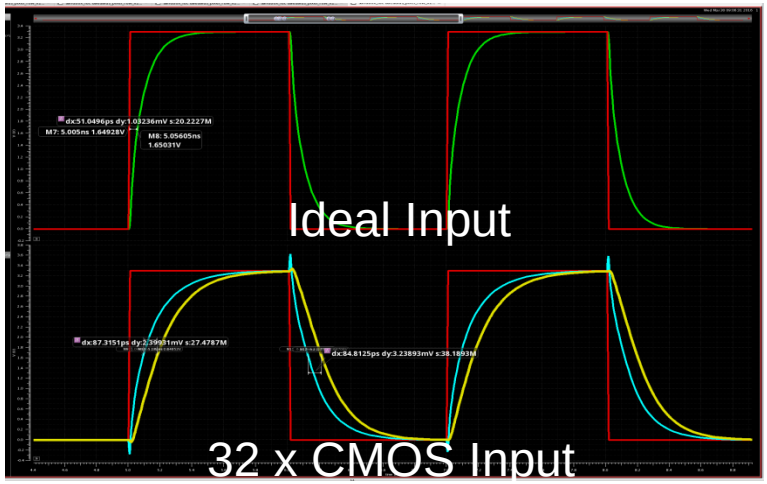


Active array size: 12.8 mm x 25.6 mm

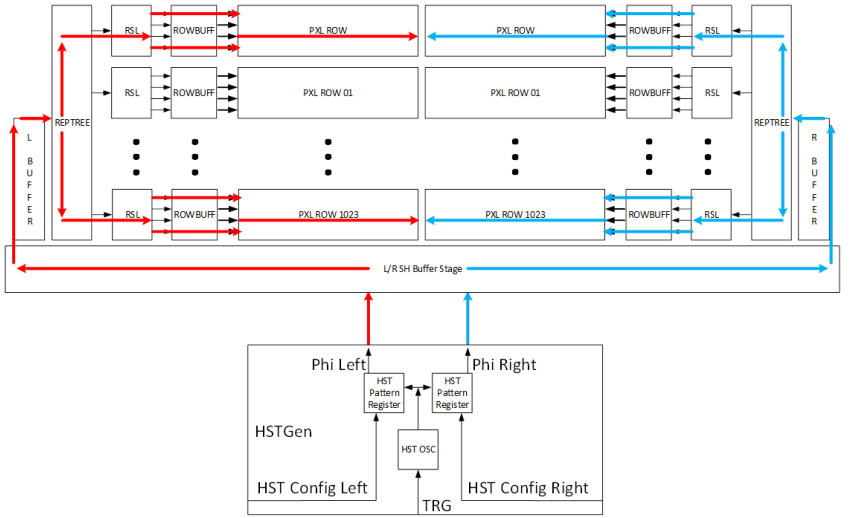
Daedalus design is well underway and we anticipate a July/August tape-out date

Sandia National Laboratories

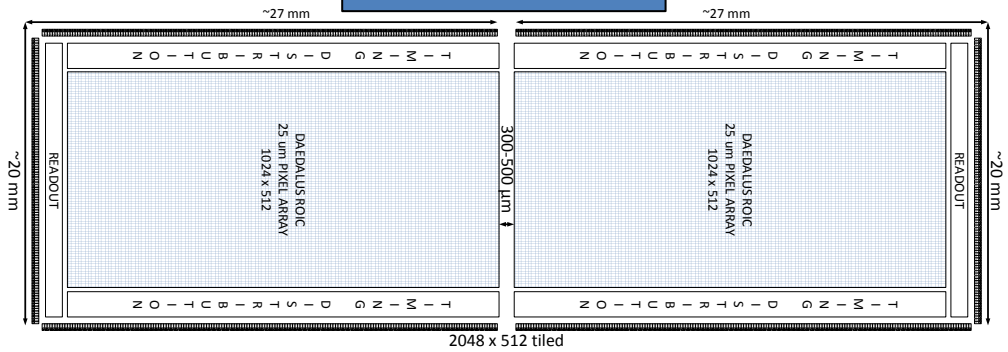
Daedalus 1 ns Row Shutter Timing Parasitic Sim



Daedalus Shutter Timing Concept



Tiled Imager Concept



Active array size: 12.8 mm x 51.2 mm

Mixed Signal ASIC/SoC

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Sandia National Laboratories

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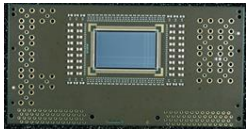
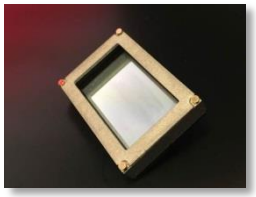
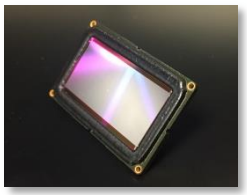
Pixel Size	25 µm x 25 µm		25 µm x 25 µm	25 µm x 25 µm	
Capacitor Full Well	1.5 million e^-		1.5 million e^-	0.5 million e^-	





TBD



Mixed Signal ASIC/SoC

Acca is a major departure in architecture/technology and will carry the program during the CMOS7 6”-8” conversion

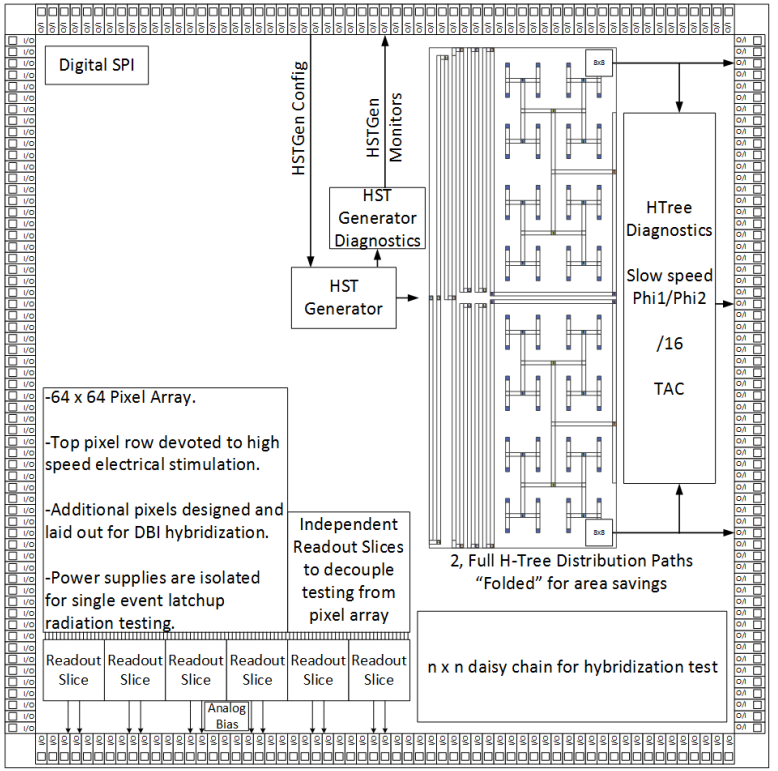
Sandia National Laboratories

- Design goals
  - **512 x 512** pixels on 25 µm pitch
  - **8 frames**
  - **< 1 ns integration time**
  - **< 1 ns inter-frame time**
  - 500 k e- full well
  - 500 e- noise floor
  - 60 dB dynamic range
- Improvements/modifications on previous ROICs
  - GF 130 nm bulk Si technology
  - CML H-tree timing distribution
  - In-pixel timing generator
  - 2-side abutable architecture
- Concerns and issues
  - Bulk vs. SOI radiation performance
  - MOSCAPs have a non-linear response and poor leakage
- Status
  - Test chip containing individual blocks of circuitry has been fabricated and is in packaging and awaiting testing

GF 130 nm Density Compared to CMOS7

	Hippogriff	Icarus	Acca (IBM)
Transistors / Pixel	12	14	148
Analog Storage	2 X 250 fF MIM	4 X 75 fF MIM	8 X 40-140 fF MOS

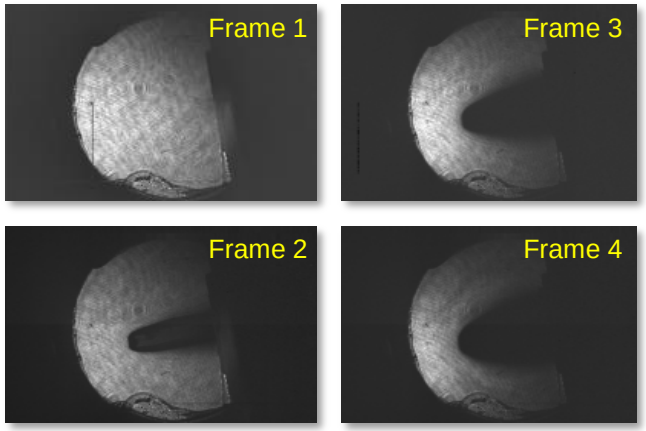
Acca Test Chip



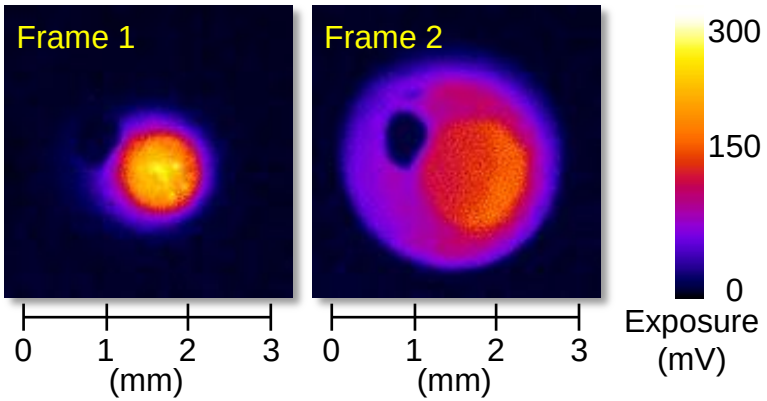
Mixed Signal ASIC/SoC

Recent results from the UXI hCMOS imagers

- Z Facility (SNL): Pecos test chamber and Magnetized Liner Internal Fusion

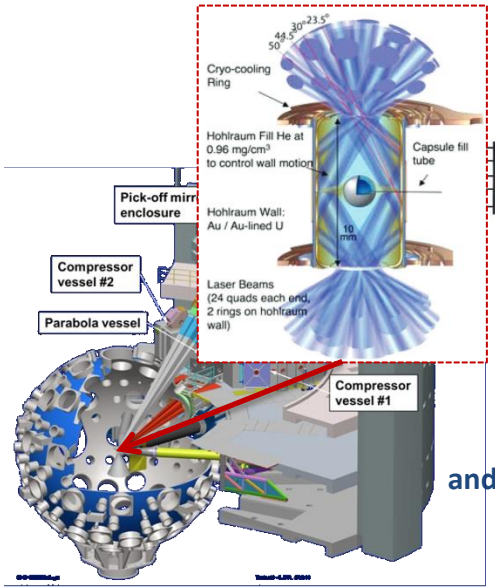


Hippogriff Gas Cell Shadowgraphs
in "Pecos" Test Chamber (4ns-4ns Timing)

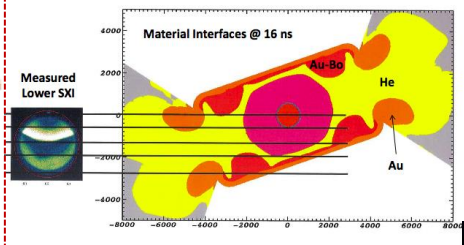


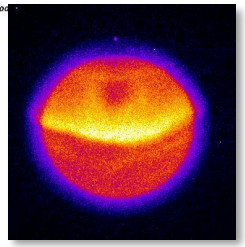
Furi Gas Cell Shadowgraphs
in Z-Machine (9ns -1ns Timing)

- NIF (LLNL): Gated Laser Entry Hole (G-LEH)

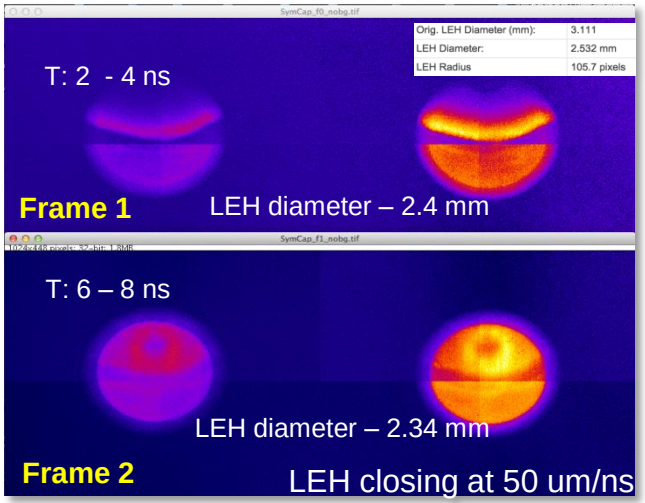


NIF Hohlraum
and LEH Viewing Angle





SXI
(Time Integrated)

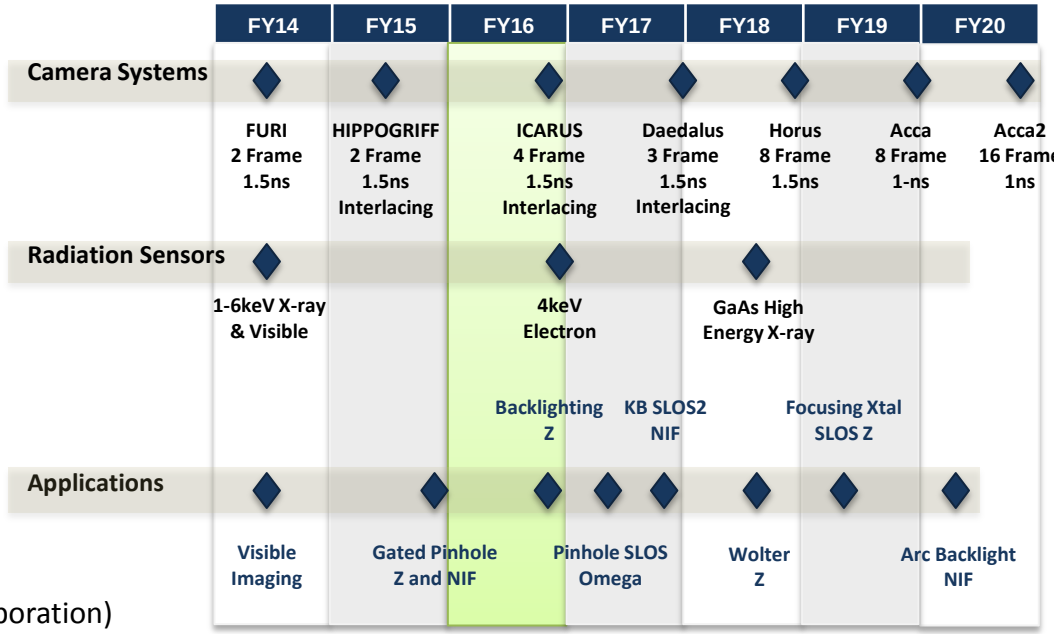


Furi Pin-Hole LEH Images
(2ns -2ns Timing)

The UXI program has created a roadmap for ROIC, detector, and camera system development that meets the needs of the National Diagnostics Initiative

Sandia National Laboratories

- Program Focus Areas
  - Existing Camera Support (Furi/Hippogriff)
    - Z-machine and NIF
    - FPA production and delivery
  - SLOS Pulse Dilation 10ps Imager
    - Collaboration with General Atomics
    - Icarus FPA system development
  - ROIC Design
    - Next generation ROICs
  - Detector Development
    - High energy X-ray detection
    - Low energy X-ray/electron (NASA collaboration)



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BACKUP

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Sandia National Laboratories

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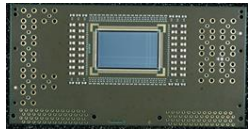
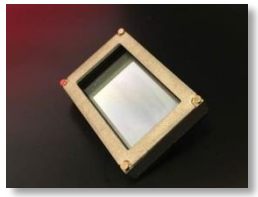
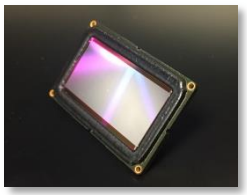




TBD



Mixed Signal ASIC/SoC

There are at least two obvious solutions to dealing with the large photocurrents a ROIC will experience under high energy fluence

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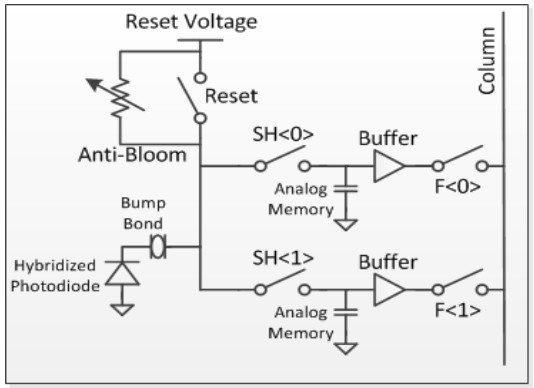
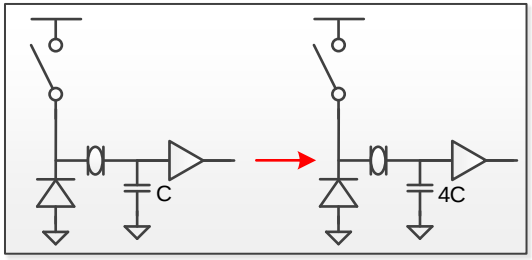
Anti-Bloom



Introduce/utilize anti-bloom transistor to compress signal at large signal levels.

(-) Might be a reasonable first candidate, however, readout circuitry begins to limit the DR with existing cameras

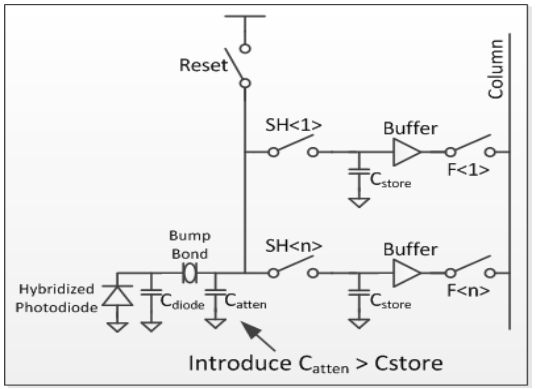
Increase Full-Well



Increase the size of the analog storage capacitor.

(+) This solution is a good candidate, however, speed and area impacts need further study

Capacitive Charge Division



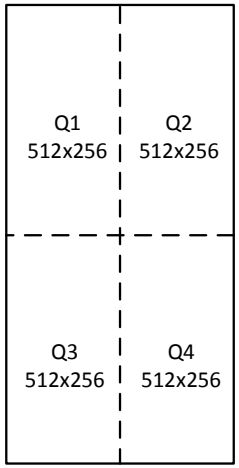
Introduce a charge dividing capacitor on the front-end of the ROIC.

(+) This solution is a good candidate, however, will need to look at impacts to reset and analog signal levels.

Horus will attempt to integrate as much capability as possible while working towards a monolithic SoC

- ROIC features
  - 1024 x 512 pixels on 25 µm pitch
  - **TBD # of frames**
  - 1 ns integration time
  - 1 ns inter-frame time
  - 60 dB dynamic range
  - **TBD e- full well**
  - 500 e- noise floor
  - Common Cathode detector
- ROIC features and iterative goals
  - Resolve any learning or suspected issues with Daedalus
  - Quadrant level independent timing
  - On chip ADCs will be investigated
  - Digital SPI interface to simply system design
  - 1 side abutable design like Daedalus

Quadrant timing Diagram



Horus Block Diagram

TBD

Multiple efforts at SNL and at other organizations are active in the realization of these FPAs and imaging systems

Sandia National Laboratories

- Sandia Efforts and Team Members
  - (MESA) Microsystems S&T & Components
    - ROIC Design/ Program Management
    - Photo-diode Design, Modeling and Testing
    - Fabrication, Packaging, Integration, and ATE Testing
    - Radiation Performance
  - Pulsed Power Sciences Center
    - Camera System Development
    - Camera System Integration
    - Camera System Testing
- National Diagnostics Initiative Partners
  - Lawrence Livermore National Labs
  - Laboratory for Laser Energetics
  - General Atomics
- Industry Partners
  - Ziptronix – 3D ROIC to detector hybridization
  - Daisho - FPA package fabrication
  - Delta/Corwil – FPA package assembly and population

The UXI program will continue to leverage the unique capabilities at MESA for the development of next generation imaging systems for an expanding ICF/HED user base

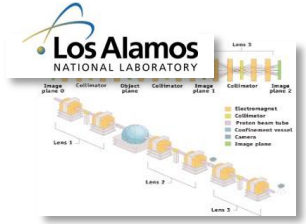
- Areas of Investment/Development
  - Integration
    - In-house DBI and Indium hybridization for CMOS7 ROICs/detectors
    - Through silicon vias for power distribution and sensor abutment
  - Boutique Detectors
    - III/V materials
    - Integrated charge gain modification / charge shunting devices
  - ROIC Design
    - High speed radiation hardened pixels (8-10 bits in ~100ns)
    - 180nm CMOS8 designs

SNL – Z-Machine

LLNL - NIF

LLE - OMEGA

New Interests !!



LANCE/MaRIE

NSTEC- Down Hole

Mixed Signal ASIC/SoC