Designing a New Master Timing Generator

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Abstract

At the Laboratory for Laser Energetics, a complex network of electronics serves to direct and monitor the operation of the OMEGA laser system. Some of these components, like the Master Timing Generator, are aging and incompatible with modern technology. The Master Timing Generator, or MTG, first introduced in the 1990s, is a logic device responsible for keeping all of the laser system triggers for diagnostic hardware such as computers, cameras, and sensors tightly synchronized to the laser pulse. To replace the present device's 20-year-old technology, a new MTG was designed on a modern Complex Programmable Logic Device chip known for its low power consumption and high reliability. An Ethernet interface was also developed so that the LLE network could communicate directly with the MTG, integrating with existing protocols and speeding error diagnosis. Oscilloscope traces verify that the up-to-date MTG faithfully reproduces all of the behaviors of its predecessor. Additionally, the device's new web page adds to its utility as LLE proceeds with its systems renewal.

1. Introduction

1.1 Master Timing Generator

The Master Timing Generator (MTG) is an input-output digital logic device that serves as a source of synchronizing signals for the thousands of laser system components in OMEGA, such as the video cameras, laser source, flash lamps, and shot diagnostics. Some of the MTG signals are generated continuously, to provide a time base or periodic reset for digital systems; others are generated in response to a stimulus from the Shot Executive to coordinate processes before, during, and after a laser shot. The Shot Executive is the computer system in the main control room responsible for coordinating all laboratory activities related to a laser shot according to the instructions from the Shot Director and other LLE staff. Located in the rear of OMEGA's Power Conditioning Office, the centrally located MTG distributes its signals via a series of cables, fiber optics and amplifiers throughout the laser bay and control room. The signals are accessible to technicians and equipment from standardized sets of ports at key locations. The MTG has four primary inputs and six primary outputs (Fig. 1), summarized below.

Continuous Inputs • 38 MHz **Gating Inputs** • T-10 Enable • T-0 Enable **Other Inputs** • Reset	**Continuous Outputs** • H-Sync • V-Sync • Five-Hz • Tenth-Hz **Gating Outputs** • T-10 • T-0

38 MHz. Known colloquially as the "heartbeat" of the LLE facility, the 38 MHz signal is an exceptionally stable sinusoidal signal used as a time base for all laboratory operations. Its actual

frequency is approximately 37.8 MHz. Its period is 26.46 ns. It is generated by a temperature-controlled, vibration-damped source, and distributed universally in the OMEGA system and the surrounding research laboratories.

T-10 Enable. The Shot Executive computer enables the MTG to assert a gated T-10 pulse with the T-10 Enable signal. The input is normally low, and is driven high by the Shot Executive for approximately 10 seconds so that it overlaps a single Tenth-Hz pulse, at which time the T-10 pulse is asserted (Fig. 2).

T-0 Enable. As for the T-10 Enable signal, the Shot Executive computer enables the MTG to assert a gated T-0 pulse with the T-0 Enable signal. The input is active high and is driven by the Shot Executive for approximately 10 seconds so that it overlaps a Tenth-Hz pulse, at which time the T-0 pulse is asserted. T-10 Enable and T-0 Enable allow the MTG to function as a synchronized intermediary between the Shot Executive and the OMEGA laser system.

Reset. The reset signal is issued by the Shot Executive, or by pressing the associated button on the MTG readout. It is active high. All outputs return to their default states for the duration of the reset pulse, and then resume normal operation on the pulse's falling edge.

H-Sync. H-Sync, or "Horizontal Synchronization," is an active-low, continuously generated periodic digital signal used exclusively by cameras. It has a frequency of approximately 58 kHz and a pulse width of 6.94 μs. The rising edges of H-Sync precede the rising edges of Tenth-Hz by 200 ns to make them coincident with V-Sync's rising edges. Because it is common to all LLE cameras, H-Sync ensures that all horizontal lines are synchronous. See Appendix A for details on analog video signals at LLE.

V-Sync. V-Sync, or "Vertical Synchronization," is an active-low, continuously generated periodic digital signal used exclusively by cameras. It has a frequency of approximately 60.2 Hz, significantly lower than H-Sync, and a pulse width of 569 μs, or 9 H-Sync cycles. The rising edges of V-Sync are always coincident with a rising edge of H-Sync. Because it is common to all LLE cameras, V-Sync ensures that all fields and frames recorded by LLE's imaging systems are synchronous. See Appendix A for details on analog video signals at LLE.

Five-Hz. Five-Hz is a continuously generated periodic digital signal primarily used to trigger human interfaces and displays to refresh at a rate comfortable for viewing. It has a period of 200 ms and a pulse width of 400 ns.

Tenth-Hz. Arguably the most important synchronization signal at LLE, the Tenth-Hz pulse is a continuously generated periodic digital signal used by instruments, computers and other equipment to trigger low-frequency tasks such as data dumps, resets and automatic self-diagnostic routines. It has a period of 10 s and a pulse width of 400 ns. The rising edges of the Tenth-Hz pulses are always precisely coincident with every 50^{th} Five-Hz pulse.

T-10. The sequence of events immediately before, during, and after irradiation of the target, occurring approximately once per hour at LLE, is known as a "shot cycle." During a shot cycle, exactly one T-10 pulse is asserted 10 seconds and 5 ms (one Tenth-Hz period and the shot delay) prior to irradiation, indicating that a shot is imminent. Upon receiving this signal, all laboratory devices initialize final preparation for the laser shot, including calibration, positioning and priming. Devices may also begin timing routines. With a pulse width of 422 ns, the T-10 pulse is identical to and occurs coincidently with a Tenth-Hz pulse.

T-0. During a shot cycle, exactly one T-0 pulse is asserted 5 ms prior to irradiation. Upon receiving this signal, laboratory devices initiate fine timing routines for triggering extremely time-sensitive instruments like streak cameras. With a pulse width of 422 ns, the T-0 pulse is identical to and occurs coincidently with a Tenth-Hz pulse.

Unlike a computer or microprocessor, the MTG does not have an internal clock signal; it is a purely combinational logic device. In general, the MTG utilizes digital counters to synthesize its continuously generated signals at integer multiples of 38 MHz. Its shot-cycle-related signals are derived from and synchronous with its continuous signals and are gated by the Shot Executive.

1.2 Rate Regenerator Modules (RRMs)

RRMs are complementary devices to the MTG in that they regenerate other relevant timing signals locally by monitoring the Tenth-Hz signal from the MTG and the laboratory-universal 38 MHz signal. RRMs are placed in strategic locations throughout OMEGA. All RRMs are slaved to the MTG, and are thus synchronized, but the signals they produce are more specialized for nearby applications and suffer from less noise due to long cabling. An RRM served as an important prototyping platform for the new MTG.

1.3 The Old MTG

The MTG currently installed in OMEGA, hereafter referred to as the "old MTG," was introduced in the 1990s (Fig. 3). At its heart is a Stamp microcontroller.

The old MTG is out of date in a variety of ways. While the industry standard for integrated circuit (IC) packaging has progressed to 0.5 mm pins or, even more recently, microdot array, the MTG continues to utilize components with tenth-inch-pin packaging. This discrepancy makes the parts difficult to replace because the ICs are no longer readily available. Its central logic device, the Stamp microcontroller, has its own set of limitations: microcontrollers have been replaced with combinational logic, such as Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs), in applications such as this one; fewer programmers are now proficient with the Stamp's programming language, BASIC; and the microcontroller's development tools are no longer produced. Many newer devices in the OMEGA system, like RRMs, have a network interface and error reporting capability, features that the old MTG markedly lacks. These issues were addressed in the design of the new MTG.

In addition to the MTG inputs and outputs listed above, the old MTG has an "Incomplete Shot" indicator LED, which illuminates under any of the following circumstances:

- T-10 Enable is brought high, then low, without overlapping a Tenth-Hz pulse.
- A Tenth-Hz pulse occurs after T-10 Enable went low, without ever receiving a T-0 Enable.
- T-0 Enable is brought high, then low, without overlapping a Tenth-Hz pulse.

All of these conditions indicate that a shot was initiated by the Shot Executive, but was aborted short of completion. This functionality was considered when designing the new MTG.

1.4 Goals

The principal aim of the work undertaken was to replicate the old MTG on a new platform. The new platform was required to be modern, so that its replacement parts would be available in case of failure and maintenance would be simpler; flexible, so that any MTG behavioral changes required in the future would be implementable on stable hardware; and industry-standard, so that the hardware and corresponding backup hardware could be manufactured without the necessity of specialty fabrication services.

Secondary goals included safeguarding, error detection, and network communication capabilities for the MTG. Safeguards against noisy environmental conditions and incorrect shot cycle signaling were implemented. Several modes of error detection were pursued and evaluated, and two were implemented, in order to increase reliability and traceability of faults: shot error and clock error. Network communication was an objective because LLE is in the midst of a laser control system update and renewal in which older components are outfitted with the means to communicate over LLE's IP network. Networking allows the MTG to report its status and error messages to querying technicians and computer systems.

2. Designing a New MTG

2.1 Complex Programmable Logic Device

A Complex Programmable Logic Device, or CPLD (Fig. 4), was chosen as the platform for the new MTG. A CPLD is a medium-complexity digital logic device with non-volatile configuration memory constructed from an array of macrocells, each of which is a gate array that can be reconfigured arbitrarily. Whereas the old MTG utilized multiple interconnected discrete integrated circuits, the CPLD is a single 20-mm-square integrated circuit. All of the logic in the old MTG was condensed into one CPLD chip. Additionally, the CPLD-based MTG can be reprogrammed to add features in the future.

The Xilinx 256-macrocell CoolRunner-II-series CPLD was used because of its low propagation delay, low power consumption and high reliability. The OMEGA laser system, being by nature a light-speed arrangement, demands exceptional timing precision on the order of tens of nanoseconds from the MTG. The 256-cell CoolRunner-II pin-to-pin delay of 5.7 ns met the application requirements. Though power consumption is not itself a significant design parameter, heat production due to power dissipation should be minimized in each component

of the OMEGA system because of the environment's temperature sensitivity. The CoolRunner-II CPLD dissipates comparatively negligible heat during continuous operation. CoolRunner-IIs are more reliable because of their low heat production. A CPLD is an excellent choice of platform for redesigning the MTG.

2.2 Reverse Engineering

The first step in redesigning the MTG was full characterization of the old MTG. A backup old MTG was connected to the laboratory 38 MHz signal, and oscilloscope traces of its outputs revealed their characteristics. Analysis of the old MTG documentation, including wiring diagrams, was also utilized.

It was deduced that the signals produced by the old MTG that are named with Hertz numbers are in fact approximations, not precise frequencies; for example, Tenth-Hz was defined by the circuit architecture as 378,000,000 counts of the heartbeat signal, or 0.1003 Hz. Consequently, the LLE facility's equipment connected to the old MTG functions on an isolated, non-standard timebase that is similar to but divergent from the universal standard for time.

The results of the old MTG characterization are summarized in Table 1.

Table 1. Output Signal Characteristics of the Old MTG

Signal	Actual Frequency	Period	Period (38 MHz cycles)	Pulse Width	Pulse Width (38 MHz cycles)
H-Sync	60.2 Hz	63.3 µs	2400	6.94 µs	264
V-Sync	15.8 kHz	16.6 ms	630,000	569 µs	21,622
Five-Hz	5.01 Hz	199.2 ms	7,560,000	400 ns	16
Tenth-Hz	0.1003 Hz	9.97 s	378,000,000	400 ns	16
T-10	--	--	--	400 ns	16
T-0	--	--	--	400 ns	16

Had the MTG counted the 38 MHz signal to the precise number of cycles necessary to produce universally consistent Five-Hz and Tenth-Hz signals, its counters would seem to be arbitrarily configured; for example, the Tenth-Hz counter would need to count to 378,000,378, an unwieldy relatively prime number. Instead, the aforementioned approximations allow for significant architectural simplifications.

2.3 Counter Nesting

Rather than count each output signal independently, the MTG may produce its outputs more efficiently using a system of nested counters. The first tier in the nested-counter architecture divides its 38 MHz clock to a “greatest common factor” (GCF) for all of its signals, which is of much lower frequency; in this system, the GCF was found to be 1200, reducing the

GCF frequency to 31.5 kHz. Because there are four signals to be counted, every additional bit used in the GCF counter saves a bit from all four counters, a best case 1:3 space-on-chip optimization. Similarly, the Tenth-Hz count is an integer multiple of the Five-Hz count, so it may use the latter signal as its increment signal instead of the GCF, effectively nesting Tenth-Hz within Five-Hz and saving yet more bits. As such, the Tenth-Hz counter need only count to 50 Five-Hz cycles as opposed to 315,000 GCF cycles. Table 2 compares the number of bits necessary to count each continuously generated signal with and without counter nesting, showing significant improvement in total required bits. By nesting counters, an optimal arrangement with the smallest number of bits may be reached (Fig. 5).

Table 2. Comparison of Counter Sizes Before and After GCF Counter Nesting

Signal	Period (38 MHz cycles)	Period Counter Bits	Period with GCF (Period/1200)	Period Counter Bits with GCF
H-Sync	2400	12	2	1
V-Sync	630,000	20	525	10
Five-Hz	7,560,000	23	6300	13
Tenth-Hz	378,000,000	29	50*	6
GCF	--	--	1200	11
Total Bits		84		41

*actually Tenth-Hz period/(1200*6300)

2.4 Pre-Loaded Kick-Through

Counter nesting comes with its own drawbacks related to propagation speed. A raw counter, clocked directly by the 38 MHz signal, is limited in its input-rise-to-output-rise speed only by the string of logic gates in the threshold comparison operation that signifies the end of its count. On a device of the speed grade possessed by CoolRunner-II CPLDs, the combinational delay is a matter of a few tens of nanoseconds, but if the counters are nested, with each counter's output signal becoming the increment signal of the next, the propagation delay is compounded. With three layers of nested counters, the combinational delay reaches a magnitude approaching the leading-edge transition time of the old MTG's signals, altering the output measurably and rendering the approach unsuitable. However, further optimization solves the propagation delay problem.

The low-level logic of each counter was specialized to minimize propagation delay. The customized counters take advantage of the relatively long time between GCF counts to prime themselves for quick signal throughput upon reaching their counter thresholds. In this report, this counter alteration will be referred to as “Pre-Loaded Kick-Through” (PLKT). When the PLKT counter reaches a count preceding its threshold by one, it sets an internal flag that denotes that the next increment signal will be the threshold. The time-consuming threshold comparison operation is finished on the previous iteration. A single AND gate, taking the flag and the increment signal as inputs, is the only contributor to propagation delay. On CoolRunner-II CPLDs, AND gates have a standard delay of 1.2 ns, making counters implementing PLKT an

order of magnitude faster than standard counters. Combining nested counters with PLKT, it is possible to generate trigger signals of the correct frequency and with acceptably low delay.

2.5 Triggered Pulsers

In order to recreate the pulse widths of the old MTG, another logic component was developed. Though no OMEGA system device relies on the MTG pulses to be of precise duration, an effort was made to replicate this aspect of the old MTG in order to maximize compatibility. The component, here called a "Triggered Pulser," accepts a trigger input from one of the PLKT counters and outputs a signal that stays high for a specified number of 38 MHz cycles. These counter thresholds are hard-programmed to give precise, uniform pulse widths consistent with the old MTG. They are easily reconfigurable with each code download. Triggered Pulsers enhance modularity, ease of update, and similarity to the old MTG.

A variation on the Triggered Pulser, the Delayed Pulser, was also developed for V-Sync and H-Sync. It accepts a trigger input from a counter, waits for a specified number of 38 MHz cycles, and then outputs a signal that stays high for another specified number of cycles. Both V-Sync and H-Sync must be synchronized with the laser pulse, which occurs 5 ms after T-0. V-Sync was delayed the full 5 ms, since its period is longer than 5 ms, while H-Sync was delayed only enough to make it coincident with V-Sync.

2.6 Qualitative Plan

In summary, the qualitative circuit architecture for the continuous outputs is as shown in Fig. 6: the 38 MHz signal is divided by 1200 by a GCF clock divider. The divided clock becomes the increment signal for three counters implementing PLKT: V-Sync Trigger, H-Sync Trigger, and Five-Hz Trigger, which count to preset relatively prime thresholds of 6300, 2, and 525 respectively and reset continuously. The output of the Five-Hz trigger is directed to an additional PLKT counter, Tenth-Hz Trigger, with threshold 50. The first two trigger signals are inputs to two Delayed Pulsers for the actual V-Sync and H-Sync, which produce pulses of duration 264 and 21,622 38 MHz cycles, respectively. The second two trigger signals are inputs to two Triggered Pulsers for the actual Five-Hz and Tenth-Hz outputs, which both produce pulses of duration 16 38 MHz cycles. The T-10 and T-0 outputs are simply the Tenth-Hz pulses gated by T-10 Enable and T-0 Enable.

3. Implementation

3.1 Simplified Test Setup

The first steps toward implementation of the MTG took place on a Xilinx CoolRunner-II CPLD Demo Board (Fig. 7). The full architecture was implemented in VHSIC *(Very-High-Speed Integrated Circuit)* Hardware Description Language (VHDL) code. Unlike procedural programming languages, VHDL describes the way in which circuit elements in the macrocells of the CPLD will be physically connected. One attribute of VHDL, called "generic," allowed the design of modular logic components such as PLKT counters and Triggered Pulsers on general terms so that they could be reused with different thresholds, configurations, and relationships to other components.

All four continuous outputs were routed to LEDs embedded in the demo board. Reset functionality, which restarted the CPLD with cleared counters and reinitialized signals, was added and associated with a pushbutton on the demo board. For testing, a 1 MHz quartz crystal oscillator was used for a clock in place of the laboratory 38 MHz (slowed to 2.6% frequency) so that the signals would be observable. A few measurements with a stopwatch and a brief proportional calculation verified that the continuous signals had the correct frequencies, given their slow input clock.

3.2 RRM Test Setup

An RRM was chosen as the best test setup for the MTG because it contains a similar CPLD, it shares many of the MTG's I/O requirements, it is readily available, and it is convenient to reprogram. The VHDL code was migrated and mapped to the RRM's logic device, a CoolRunner-II 384-macrocell CPLD. A pulse generator set at 37.8 MHz was connected to the RRM's clock input to simulate the laboratory 38 MHz; its output pins were connected to a breakout board for oscilloscope probing (Fig. 8). Oscilloscope measurements of V-Sync, H-Sync, Five-Hz and Tenth-Hz were taken and compared with the specifications obtained through reverse engineering. The new MTG was found meet the specifications derived from the old MTG to an acceptable tolerance, as summarized in Table 3. In the table, the "expected" value is the specification value converted into the units of the measurement.

Table 3. Continuous Output Signal Test Results and Comparison with Specifications

Five-Hz Signal				
Characteristic	Specification	Expected	Measured	**% Difference**
Period	7560000 clks	199.2 ms	199.9 ms	**0.35%**
Pulse width	422 ns	422 ns	449.8 ns	**6.59%**

Tenth-Hz Signal				
Characteristic	Specification	Expected	Measured	**% Difference**
Period	378000000 clks	9.97 s	10.00 s	**0.30%**
Pulse width	422 ns	422 ns	449.8 ns	**6.59%**

H-Sync Signal				
Characteristic	Specification	Expected	Measured	**% Difference**
Period	2400 clks	63.3 µs	63.46 µs	**0.25%**
Pulse width	6.94 µs	6.94 µs	6.982 µs	**0.61%**

V-Sync Signal				
Characteristic	Specification	Expected	Measured	**% Difference**
Period	630000 clks	16.6 ms	16.66 ms	**0.36%**
Pulse width	569 µs	569 µs	571.9 µs	**0.51%**
Delay after T-0	5.00 ms	5.00 ms	5.00 ms	**0%**

Additionally, the Five-Hz and Tenth-Hz signals were shown to have coincident rise times within 1.3 ns, and V-Sync and H-Sync were shown to have coincident rise times within 1.2 ns (Fig. 9), both of which are tolerably low compared with the rise times of the pulses.

The RRM test setup allowed for an expanded testing scheme; its extra inputs allowed the gated signals to be tested as well. A Shot Cycle Simulator (SCS) device, which outputs the same sequence of T-10 and T-0 enable signals as the Shot Executive, was connected (Fig. 10). The MTG was verified to produce synchronous T-10 and T-0 signals correctly and reliably as it interacted with the SCS according to the description of the shot cycle: an active T-10 Enable was shown to produce one T-10 pulse, and an active T-0 Enable was shown to produce a T-0 pulse ten seconds later (Fig. 11). Additionally, T-10 and T-0 were each measured to have rise times coincident with Tenth-Hz within 2 ns.

3.3 Laser Shot Simulation Test

One integrated test was undertaken which would prove the correct operation of as many parts of the system as possible, short of installation at LLE. The MTG prototype was connected to a monitor, a camera, an LED, and an oscilloscope. V-Sync and H-Sync were routed to the corresponding inputs on a video signal generator. The video signal generator was in turn connected to a CRT monitor and an analog camera. It was verified that the video signal generator was synchronous with the MTG by slightly altering the setting of the frequency generator acting as a clock signal for the MTG and listening for the change in pitch of the hum produced by the CRT monitor. The camera was mounted on a workbench and connected to the monitor, where a live video feed was visible. An LED was spliced into the MTG's Five-Hz channel to simulate the laser flash. Five-Hz was chosen because it recurs quickly enough for easy observation and it had already been proven to be synchronous with T-0, the actual laser trigger, by earlier tests. The LED was pointed directly into the camera at close range, and the camera and LED were optically isolated with dark fabric (Fig. 12).

Simply capturing an image from the camera and displaying it on the CRT demonstrated that the video-related MTG signals were formed correctly. V-Sync, H-Sync, Five-Hz, and the camera output signal were probed with the oscilloscope (Fig. 13); the trace showed that the LED laser flash produced a large increase in the intensity of the camera output signal over the next two fields of video, constituting one frame (see Appendix A for details of analog video at LLE). Had the camera been asynchronous with the LED, at the incorrect frequency, the LED flash and the intensity spike would have exhibited a beat; had the timing of the LED flash been correct in frequency but incorrect in phase, the intensity spike would have been spread across two frames, or four fields. Neither of these indicators of error was apparent. Though the 5 ms delay between T-0 or, in this case, Five-Hz, and target irradiation was not included in this test, the delay between the LED pulse and the next camera blanking signal following V-Sync was measured to be 5.00 ms. The test demonstrates the correct phase and frequency relationships between the output signals of the MTG for practical use. The system was shown to be suitable for timing the OMEGA laser system.

4. Expanding the MTG

4.1 Shot Error

Though the functionality of the old MTG in the OMEGA system had been replicated and verified, the Incomplete Shot indicator LED on the old MTG had not been replaced. The Incomplete Shot represented only a small subset of possible errors, so the concept was generalized to Shot Error, including all plausible errors in the progression of the Shot Cycle. The process was tabulated using a Finite State Machine (FSM), which kept track of the Shot Cycle's state at any given time by monitoring the concerned signals: Tenth-Hz, T-10 Enable, and T-0 Enable. A correct path from state to state through the FSM was defined, and deviation from the correct path was considered error.

Five states were necessary to encode the entirety of the correct shot cycle path, as shown in the FSM state transition table (Fig. 14). In the Idle state, the MTG waits for a shot cycle to begin. When T-10 Enable becomes activated, the FSM enters T-10 Enabled. After Tenth-Hz has gone high and a T-10 pulse has been asserted, the FSM transitions to T-10 Finished. The same process recurs for T-0 Enabled and T-0 Finished, substituting T-0 Enable and T-0. Finally, when the T-0 Enable signal is no longer asserted, the FSM returns to the Idle state.

Transitions that violate the explicitly defined expected sequence trigger an error flag. For instance, it is possible that a malfunction in the Shot Executive system could cause T-10 Enable and T-0 Enable to be active simultaneously at the time of a Tenth-Hz pulse (Fig. 15), a very serious error. In order for this condition to come about, T-0 Enable must become active while the FSM is in the T-10 Enabled state, resulting in an error according to the state transition table.

Custom VHDL types were defined to implement the FSM on the CPLD, and reset-to-Idle capability was integrated with the usual reset for the MTG. The FSM does not interact in any way with the operation of the MTG; it is physically separated from the CPLD macrocells concerned with timing to improve resilience to failure. Its only output is the error information.

The Shot Error was successfully tested. An LED was used to indicate the error flag's state on the MTG prototype. The shot cycle simulator and oscilloscope were connected as in previous tests, and the LED did not light as correct shot cycles were executed. Then, each enable signal in turn was interrupted during the shot cycle, and the LED lit each time. The T-10 and T-0 Enable signals were also interchanged, which immediately caused the LED to light.

Because each FSM state is uniquely associated with a particular stage in the Shot Cycle, the errors are also unique to particular failures. This feature opens up the possibility of specific, cause-explicit error reporting. A half-byte error code was associated with each possible error in the FSM code in anticipation of this application, and cause-explicit error reporting was explored after the network interface was in place.

4.2 Clock Error

The 38 MHz signal is vital for all shot-related operations at LLE, and failure of this signal ought to be reported by the MTG because it is the hub of all timing processes. This functionality, Clock Error, was added to sense catastrophic loss of the signal and to report it to the Shot Executive. Sensing loss of 38 MHz with the MTG is non-trivial, because it acts as the

clock signal for the MTG. Combinational logic halts and the CPLD has no means of triggering self-diagnostics in the absence of its clock; it simply remains unresponsive. Nevertheless, the modular, flexible nature of CPLD macrocells provided a solution.

An external 10 kHz quartz crystal oscillator acted as both an external stimulus and a metric to which the 38 MHz signal was compared. Roughly 3800 cycles of the 38 MHz signal are expected to occur for each 10 kHz cycle; this count was checked using the "strobing" technique (Fig. 16). A counter for the 38 MHz signal was added in VHDL. Each rising edge of the 10 kHz signal caused the 38 MHz counter to pause momentarily. During the pause, the 38 MHz counter value was compared with the approximate expected value of 3800. If it deviated from 3800 too greatly, or if it was zero, a clock error was flagged. Then, the 38 MHz counter was reset in preparation for another comparison on the next 10 kHz rising edge. In this way, the 38 MHz counter was "strobed" for errors by the external oscillator.

Since the two timing signals are independently generated, the counter value at the time it is strobed must vary by at least one due to the lack of correlation between the signals. Noise can also introduce some variation in the count. To compensate, some tolerance was given to the count comparator by disregarding several of the least significant bits. Using a sequence of downloads and varying the number of disregarded bits between 1 and 10, a binary search was performed to find the minimum number of bits disregarded before stable, noise-resistant operation was achieved. The minimum was found to be four.

Like Shot Error, Clock Error sets an internal error flag when the strobe test fails. The error flag was routed to an LED on the MTG prototype. With four least significant bits ignored, the Clock Error ran for four hours continuously with no errors logged, but lit the indicator LED immediately upon disconnection of the 38 MHz signal.

4.3 Network Interface

LLE's IP network is a powerful tool through which its equipment is increasingly interconnected for ease of use and consistency of communication standards. Technicians may connect to any network-enabled device and check its status and error information from any LLE computer at will, and devices like the RRM modules have already proven the utility of such capability. The MTG was outfitted with a network interface in order to confer these benefits immediately upon installation. Error flags, error codes, reset commands, input-output information and a command line were made available over the network.

A NetBurner module was used as a communication engine for connecting the MTG to the LLE network (Fig. 17). The module is capable of both Ethernet and basic I/O communication. It can host its own webpage, and it comes with a device-specific C++-based software development kit. After assigning the NetBurner a unique LLE IP address, four bits of I/O were connected between the MTG prototype and the NetBurner. Three were assigned as inputs to the NetBurner: one to indicate Clock Error, and two to demonstrate a limited set of error codes from Shot Error. The last I/O bit was assigned as a NetBurner output, used for remotely resetting the MTG.

A webpage from an unrelated network-enabled LLE system component was adapted to display the error information and to interact with the remote reset. The two bits of Shot Error were interpreted together as a two-bit error code (range of 0-3 decimal), signifying three different sample errors (the fourth signifying no error), and formatted to display the

corresponding error messages on the webpage. The remote reset was implemented as a check-box. A command-line interface to the NetBurner was also made available for future expansion, should more sophisticated communication between the NetBurner and the MTG be established. All features are accessible in a single browser window (Fig. 18).

Using an LLE computer, the webpage was successfully accessed and displayed. Oscilloscope traces verified that the MTG underwent a reset as intended in response to the check-box interface. Using the SCS, shot errors were simulated by disconnecting the T-10 and T-0 Enable signals; the correct sample error message was displayed on the webpage each time.

5. Future Development

The work summarized herein represents only the initial stages of a longer process to update the MTG to meet new standards of reliability, interactivity and utility. Many concepts have been proven feasible, but few are ready for deployment. The LLE engineering staff will use this work as a foundation for further expansion as they prepare it for final packaging and installation. The network interface in particular has many more possibilities, such as automatic communication with the Shot Executive about status and errors, remote fine adjustment of the MTG's outputs for synchronization with OMEGA EP, and command-line routines for self-diagnosis and other functions. LLE can anticipate smoother operation, simpler maintenance, higher reliability, and tighter integration with the OMEGA system from its MTG in the future.

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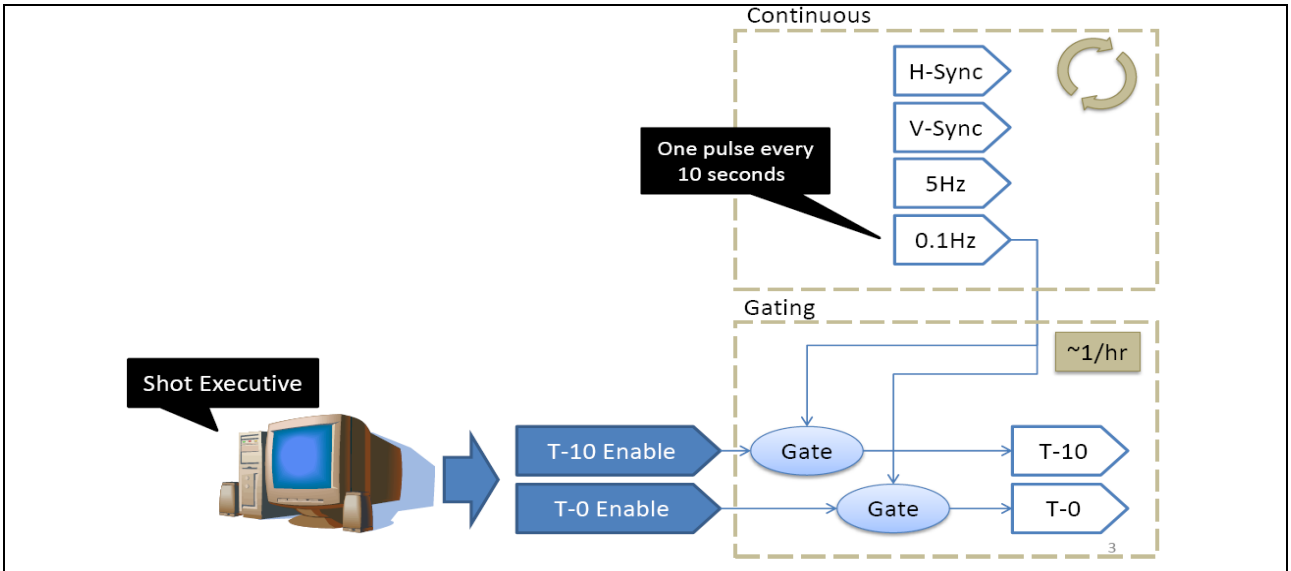

Fig. 1 Diagram of MTG Outputs: Outputs split into two groups: continuous and gating. Continuous outputs (H-sync, V-sync, Five-Hz and Tenth-Hz) are used to synchronize cameras and local timing for all devices in the OMEGA laser system. Gating outputs are only active approximately once per hour, on the OMEGA shot cycle schedule, when the Shot Executive computer system asserts T-10 and T-0 enables.

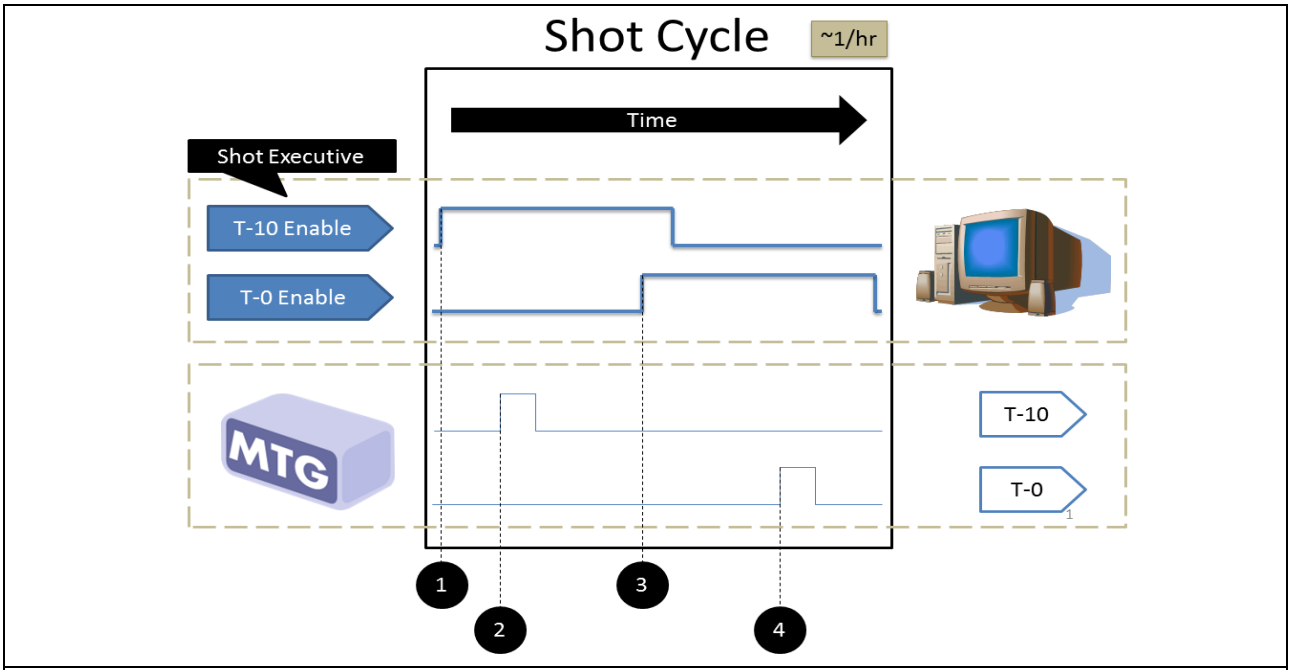

Fig. 2 Shot Cycle: In the seconds before a shot, the Shot Executive first asserts the T-10 Enable signal (1). The MTG waits for its own Tenth-Hz pulse, and then synchronously outputs the T-10 pulse (2). A few seconds later, the Shot Executive asserts the T-0 Enable signal and lowers T-10 Enable (3). The MTG again waits for its own Tenth-Hz pulse, and then synchronously outputs the T-0 pulse (4). *Pulse widths not to scale.*

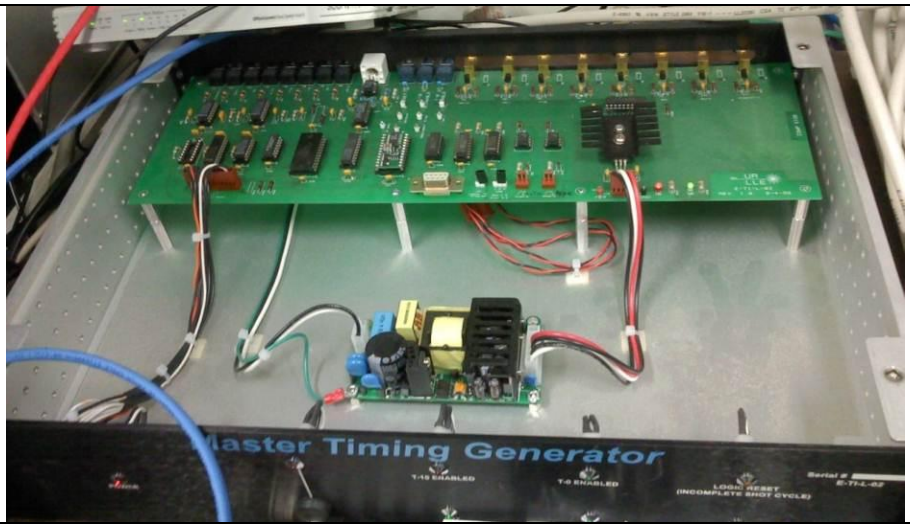

Fig. 3 Old MTG, internal view: Obsolete components and a sparse readout.

Fig. 4 CPLD: Made by Xilinx, this CoolRunner-II CPLD consumes very little power, has a very low pin-to-pin delay, and measures only 20 mm x 20 mm.

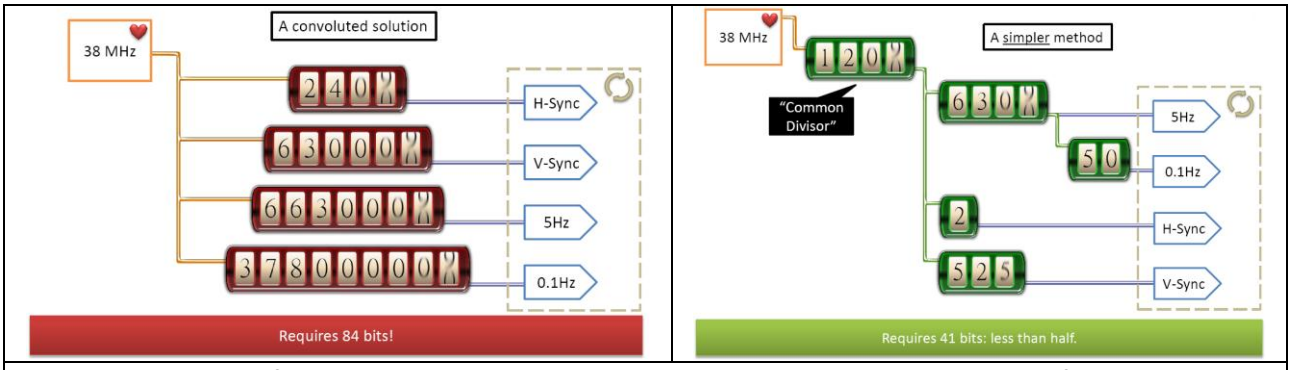

Fig. 5 Comparison of counter designs: Two possible counter arrangements are shown for dividing the heartbeat signal. The first uses one counter per signal. The second uses counters to count the outputs of others. By nesting counters, computing resources are saved.

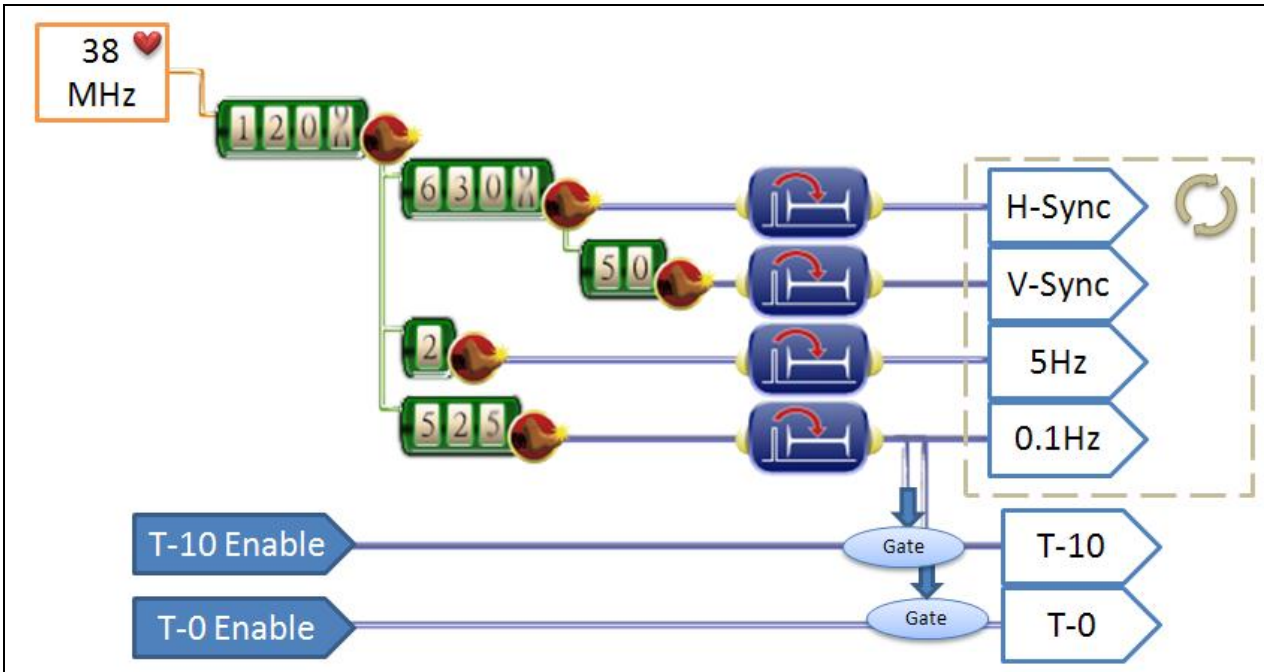

Fig. 6 Final schematic diagram: 38 MHz heartbeat divided by a cascade of nested counters, each implementing Pre-Loaded Kick-Through (red circles with boots). Triggered counters (rounded dark-blue rectangles) become outputs. Gated signals are created from Tenth-Hz output.

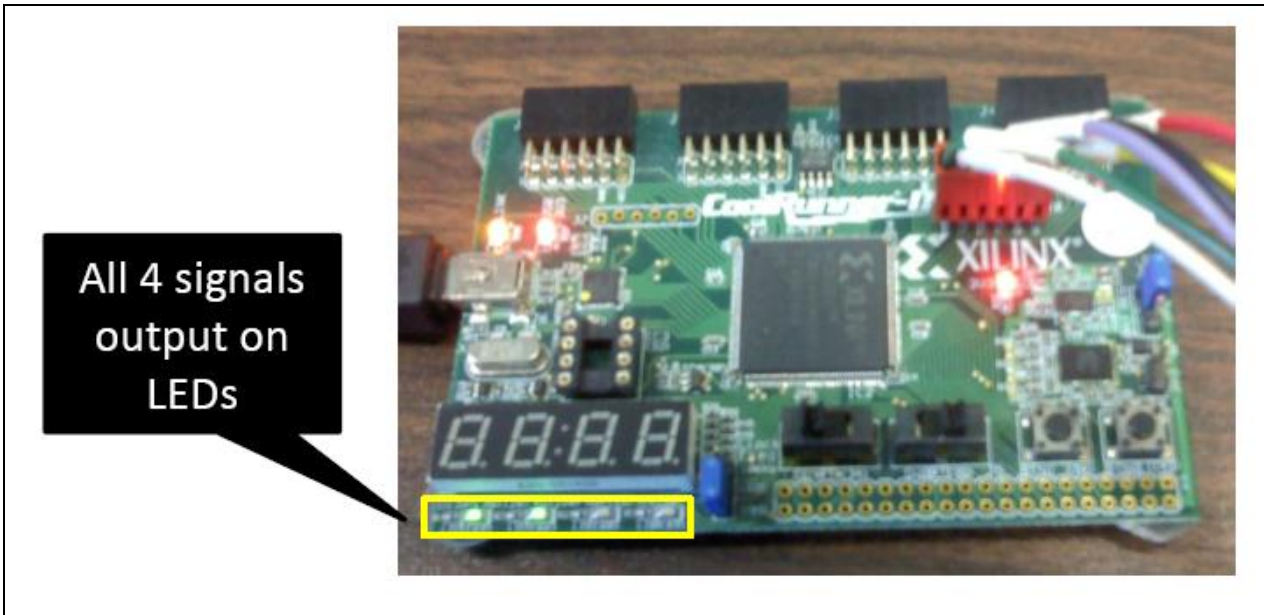

Fig. 7 Demo board with MTG program: The new MTG program was first implemented on a CPLD demo board. The four continuous outputs, V-Sync, H-Sync, Five-Hz, and Tenth-Hz, are routed to LEDs.

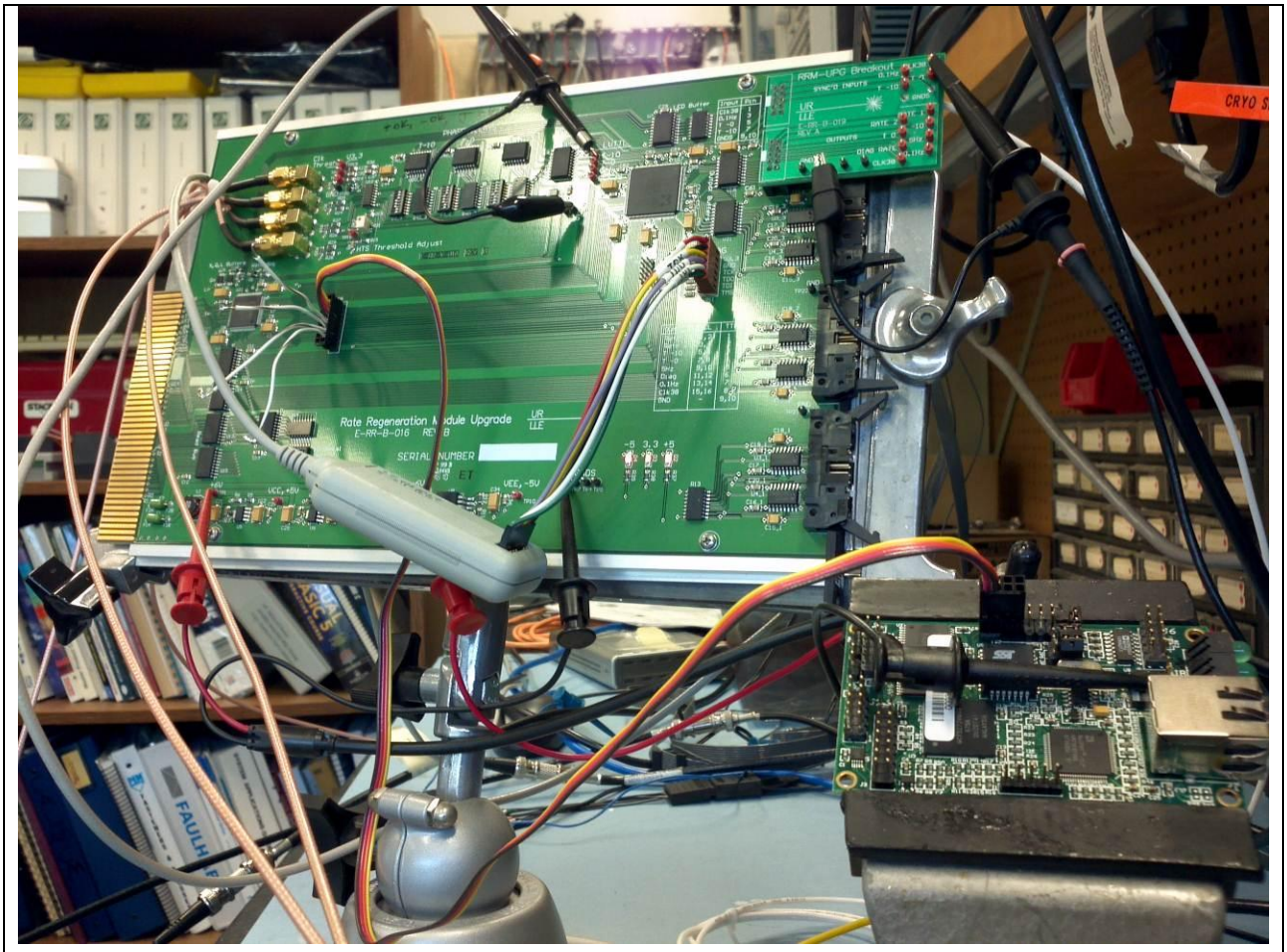

Fig. 8 Final test setup: The large circuit board is the RRM, adapted for MTG testing. Four RF-capable inputs are shown at the top left of the RRM, connected to gold-colored contacts. The V-Sync, H-Sync, Five-Hz, Tenth-Hz, T-10 and T-0 outputs are visible at the top right of the RRM, on a smaller green board, with an oscilloscope probe. The NetBurner module is shown in the lower right. The four-conductor ribbon cable (yellow, orange, red, black) is the I/0 for communications between the RRM and the NetBurner. The gray plastic device connected to the RRM via a bundle of colorful wires is the JTAG reprogramming interface for the CPLD.

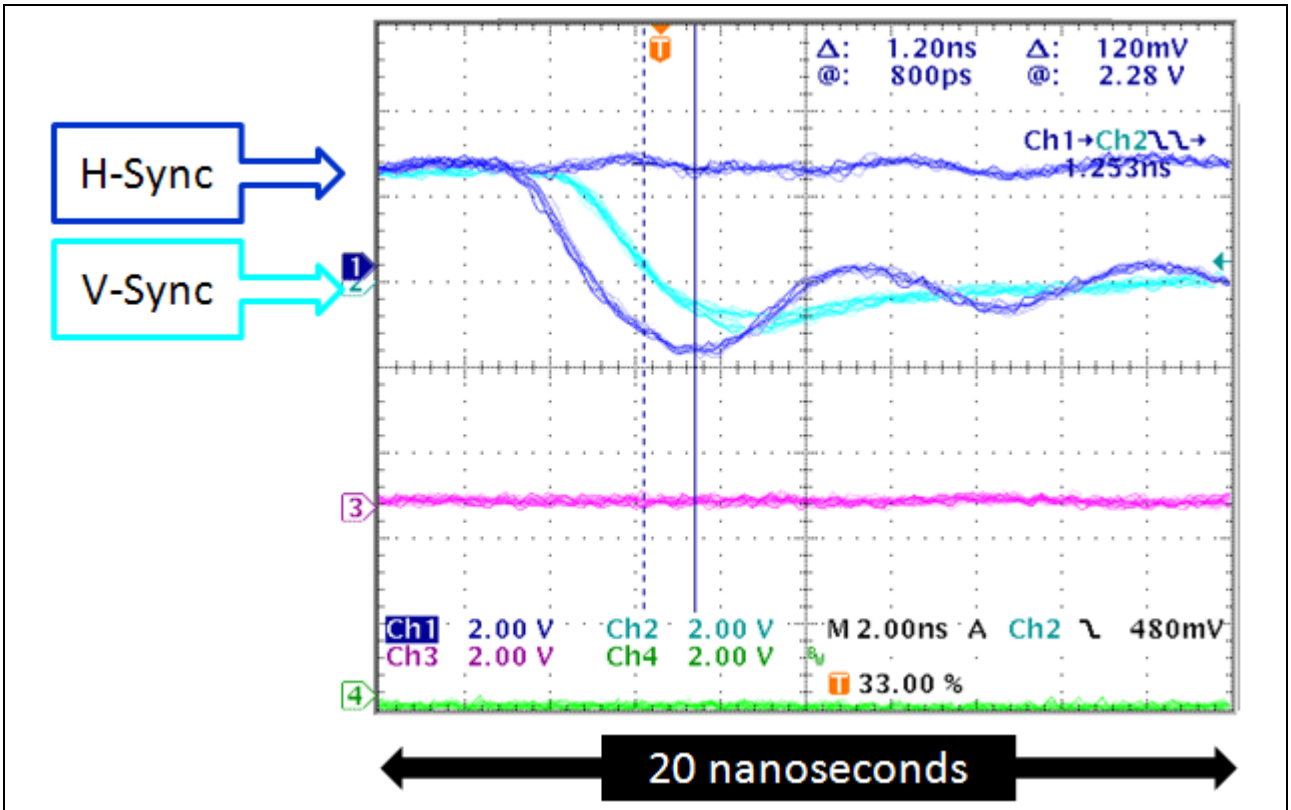

Fig. 9 Oscilloscope trace of Pre-Loaded Kick-Through results: V-Sync and H-sync were implemented using PLKT counters. V-Sync and H-Sync falling edges are shown on an extremely short time base. An exceptionally short delay of 1.253 ns is measured between edges. The result is significant because V-Sync follows H-Sync much more closely than would be possible using counters without PLKT. *Note: H-Sync appears to branch into two traces because interlaced video requires that the sync pulses only line up on every other V-Sync. Only the lower H-Sync trace is relevant.*

Fig. 10 Shot Cycle Simulator: Creates T-10 and T-0 enable pulses to imitate shot cycle progression. Connected to inputs of the RRM.

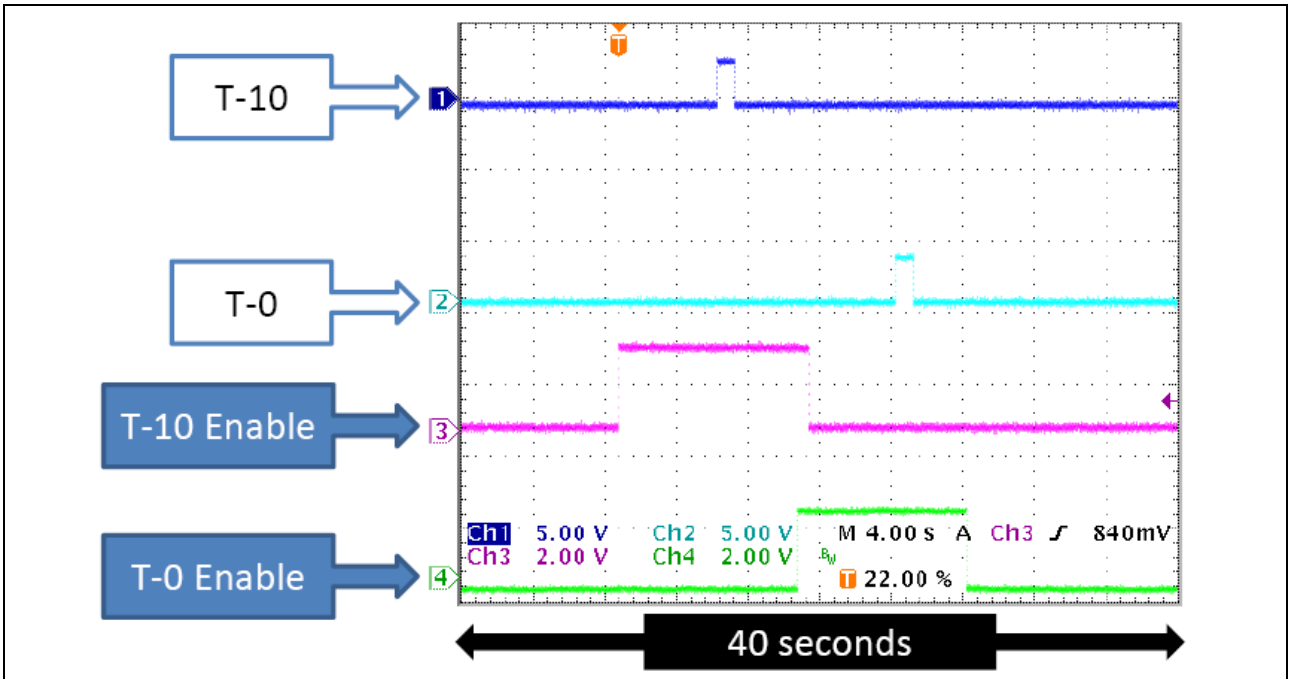

Fig. 11 Oscilloscope trace of shot cycle simulator: Correct T-10 and T-0 Enable cycle shown on channels 3 and 4, with corresponding T-10 and T-0 outputs from MTG on channels 1 and 2. T-10 and T-0 pulses were lengthened to 1.0 s in CPLD code for clarity.

Fig. 12 Synchronous camera test setup: Red LED, left image center, pulsed on T-0 to simulate the OMEGA laser. LED points directly into camera, synchronized by V-Sync and H-Sync. Setup is isolated from room light to create contrast with LED light.

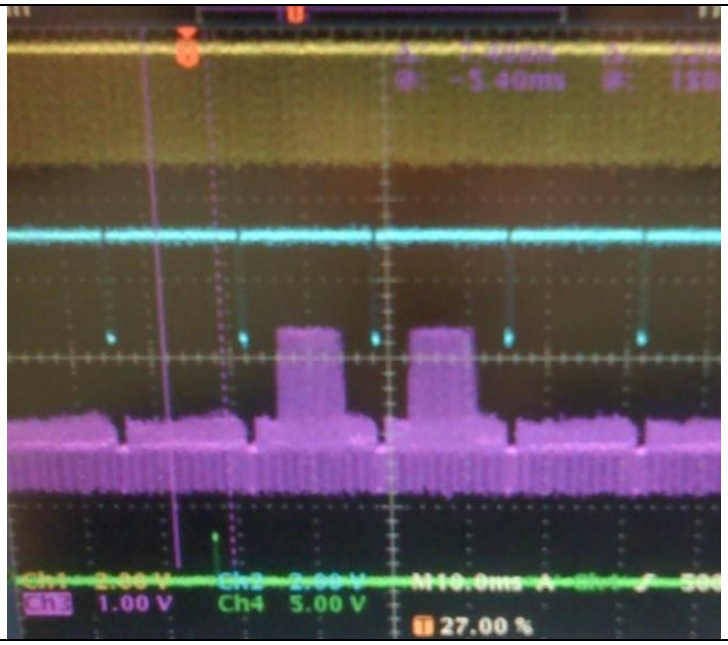

Fig. 13 Oscilloscope trace of synchronous camera test: Signals from top: H-Sync, yellow; V-Sync, blue; camera output, purple; T-0, green. The short LED pulse is shown in green near the bottom left. Since the camera uses interlaced video mode, each frame is represented by two V-Sync pulses. The next frame after the LED pulse shows spike in camera signal, or light intensity.

	T-10 Enable		T-0 Enable		0.1Hz	
state	enabled	disabled	enabled	disabled	high	low
"Idle"	Go to **"T-10 Enabled"**		error			
"T-10 Enabled"		error	error		Go to **"T-10 Finished"**	
"T-10 Finished"			Go to **"T-0 Enabled"**		error	
"T-0 Enabled"	error if 0.1Hz high			error	Go to **"T-0 Finished"**	
"T-0 Finished"				Go to **"Idle"**	error	

Fig. 14 Shot error state machine: As a shot progresses, the MTG advances through a Finite State Machine (FSM), evaluated on every clock cycle. States are shown on the left in order. The three signals relevant to the shot cycle process are shown at top: T-10 Enable, T-0 Enable, and Tenth-Hz. A white cell indicates no change, remaining in the current state. Each light green cell indicates an immediate switch to state shown. An error is flagged and an error code is logged whenever a red cell is encountered, allowing the mode of failure to be identified later.

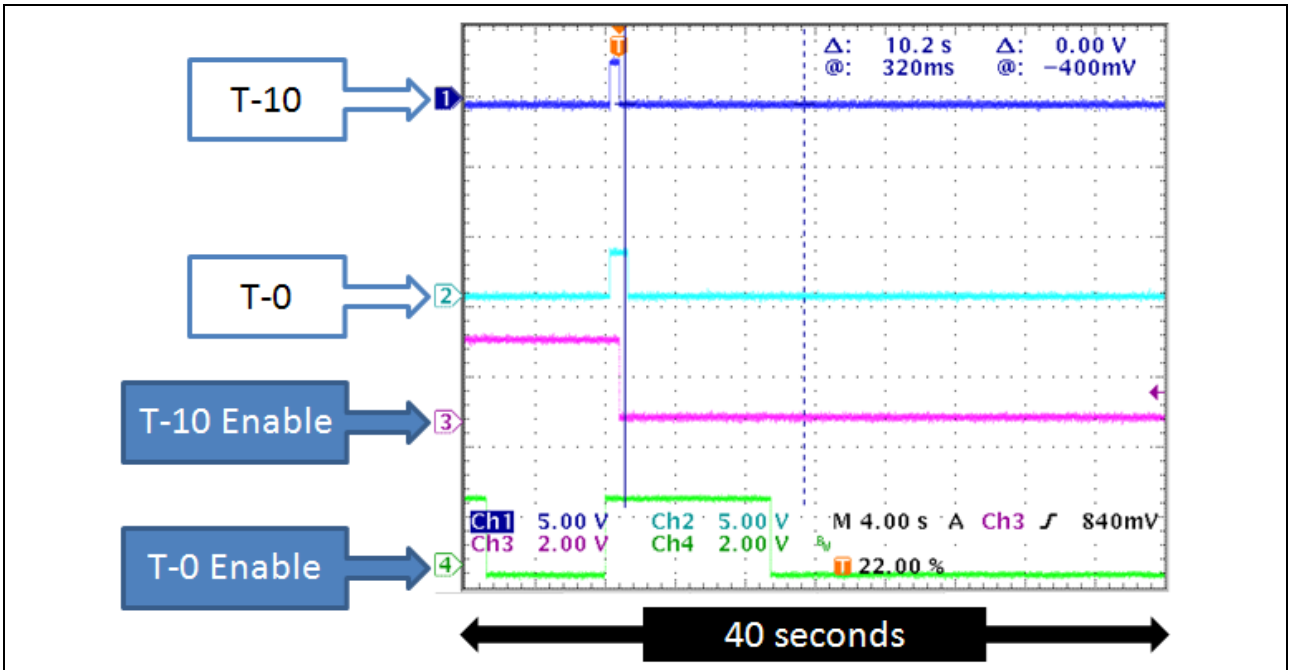

Fig. 15 Oscilloscope trace of a possible shot error: T-10 and T-0 enables overlap at the time of a Tenth-Hz pulse. T-10 and T-0 occur simultaneously as a result. An error code would be logged by the Shot Error FSM under the circumstances shown here.

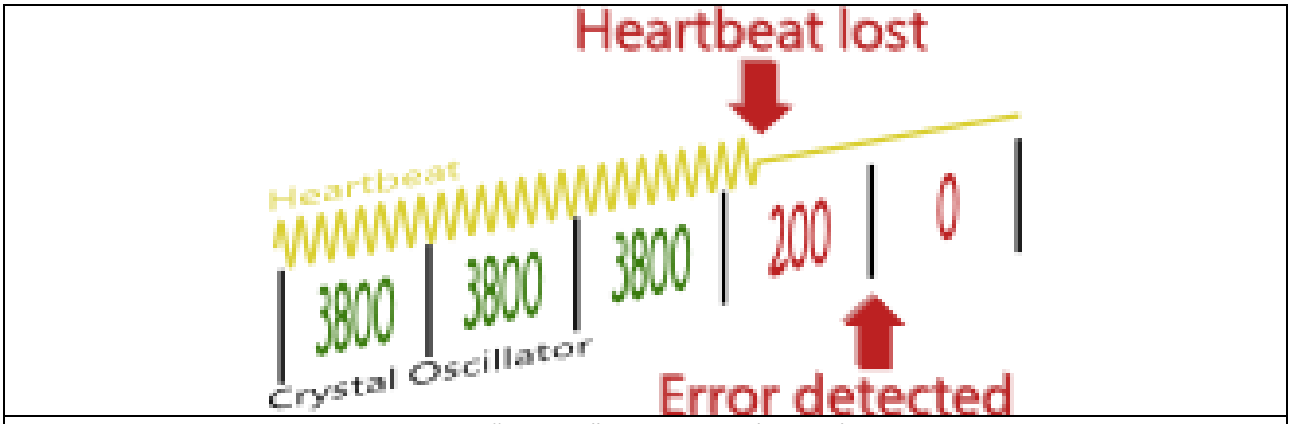

Fig. 16 Clock error: A crystal oscillator "strobes" the 38 MHz (yellow) counter on its rising edges and verifies that the counter's value lies within an acceptable range. If the counter reads too low, the clock is interrupted. If the counter reads too high, significant noise is present. In either case, the heartbeat experiences a failure, and a clock error is flagged.

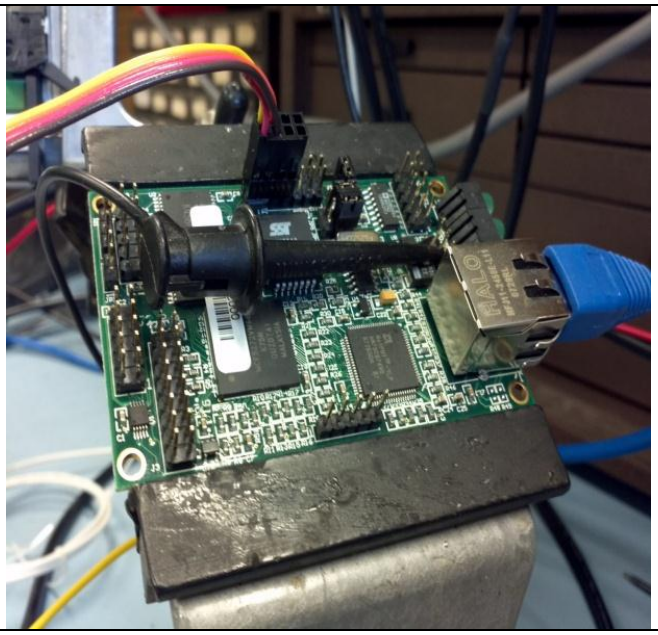

Fig. 17 NetBurner module: Shown clamped in vice. Black clip is oscilloscope probe. Ethernet port is visible in blue.

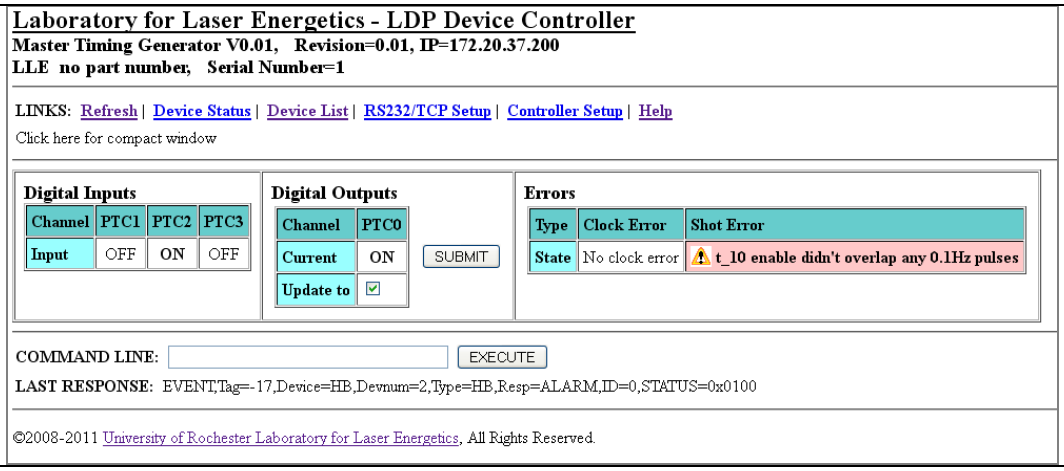

Fig. 18 MTG Webpage: Body elements, from left to right in table: digital inputs from the RRM to the NetBurner; digital output from NetBurner to RRM acting as a remote reset, shown in its default (enabled) state; error pane with formatted error messages, shown with an example error identified by the state machine: “T-10 enable didn’t overlap any Tenth-Hz pulses.” This error might occur in the case of a shot abort.

Appendix A: Analog Video at LLE

LLE makes use of analog cameras with interlaced video. These cameras output their image data serially on one conductor, one horizontal line of each field at a time. A field is all of the image data for every second horizontal line in an interlaced video feed; two consecutive fields make up a frame.

The image data are intended for use on cathode ray tube (CRT) displays. The cathode beam scans horizontal lines onto the display represented in the camera output by short (~30 µs) pulses of analog light-intensity data separated by equally short low periods (Fig. A). A "front porch," or a pause of duration equal to several horizontal line pulses, initiates transmission of a field. 525 horizontal lines are then transmitted for each field, followed by a brief "back porch," or pause at the end of the field. A "blanking period" follows, during which time the CRT display moves its cathode beam vertically to prepare for the next field.

Horizontal lines are triggered by an external "Horizontal Synchronization" pulse, and blanking is triggered by an external "Vertical Synchronization" pulse. The MTG generates these pulses, H-Sync and V-Sync. When multiple cameras are triggered by the same Horizontal and Vertical Synchronization pulses, their video feeds are synchronized and their image data are comparable in post-analysis because they were acquired simultaneously.

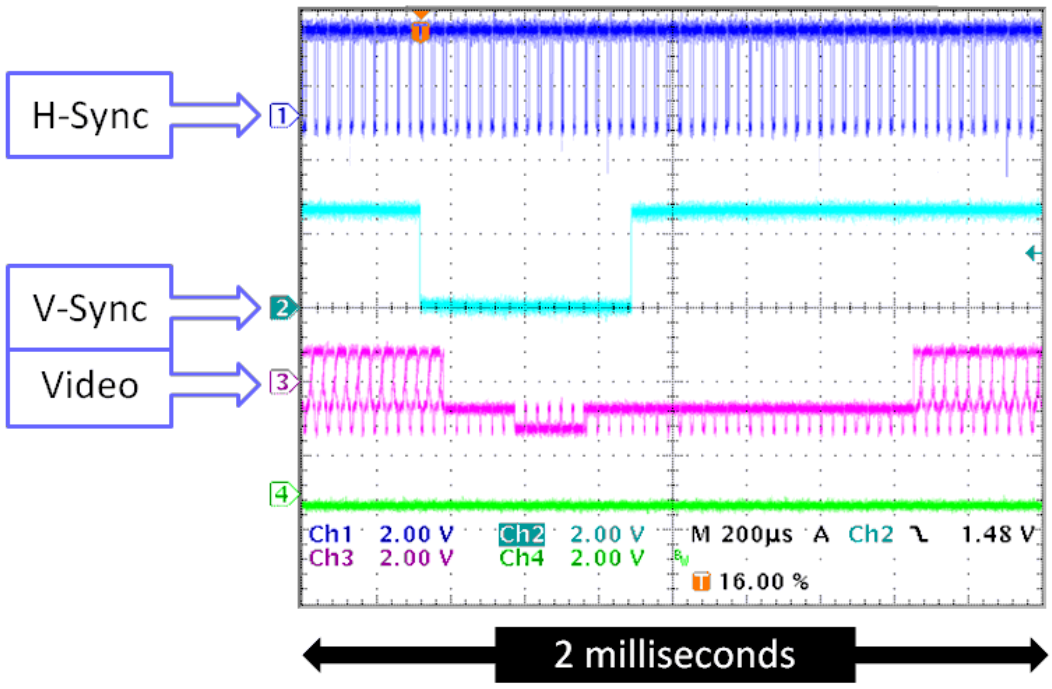

Fig. A Synchronized Video: The MTG test setup provides timing information to a camera. H-Sync is responsible for synchronizing the 525 lines in each video frame, visible at the right and left edges of the video signal. In order, the back porch, blanking, and front porch portions of the video signal take place in the lowered middle section. Synchronized by V-Sync, these features signify the transition to a new video field.