Integrated Circuit Tester Using Interferometric Imaging

A noninvasive optical diagnostic technique for testing the electrical state of an integrated circuit has been developed at LLE. The interferometric probe is capable of distinguishing between the on- and off-state of an *N*-channel field-effect transistor (FET) with micron-size dimensions. Continued development of advanced semiconductor devices relies on the availability of diagnostic techniques to identify and eliminate design flaws. As semiconductor integrated circuits (IC) become faster and more complex, they are starting to exceed the capabilities of the present generation of diagnostic probes.[1] The technique described here requires no external leads to probe the voltage state; thus, it is relatively noninvasive. A subband-gap optical pulse is used as the probe so we can look at both buried structures and flip-chip devices. The temporal resolution is determined by the duration of the optical pulse, which is in the picosecond regime. With appropriate optics, submicron spatial resolution can be achieved. Finally, if a pulse train from a mode-locked laser is used, the sampling rate can approach the IC's natural clock frequency.

Our interferometric imaging technique is being used to provide time-resolved diagnostics of semiconductor integrated circuits. The device under test (DUT) is placed in one arm of an interferometer and illuminated with a picosecond pulse from a subband-gap infrared laser. Even though the material is transparent, it does interact with the light probe. The laser samples local variations in the index of refraction, giving rise to an interference pattern, which we detect. The variations are caused by a number of physical phenomena including doping[2] in the material, heating due to the flow of electrical currents,[3] and changes in carrier concentrations due to injection.[4] These variations have both static and dynamic components. The dynamic components are associated with the normal device operation and are the most interesting. To separate the two components, the device is first imaged in a quiescent state (no external voltage applied), and then a second image is taken after the device enters a known voltage state. Differences between the two images determine where the local index of refraction has changed and by how much. Activation of the DUT electronic state is synchronized with the pulsed illumination source, and the time delay between the initiation of the state and the laser probe pulse allows us to take a series of images that map the time evolution of the interferogram. So long as the DUT state is stable, multiple probe pulses can be averaged to improve the signal to noise. The stability does not require that the state be static. For example, a given state can be initiated in the DUT and probed at a later time Δt. The DUT can then be reset to zero and reinitialized before the next laser pulse arrives at $T_{\text{clock}} + \Delta t$, where T_{clock} is a multiple of the clock period. A mode-locked laser typically operates at 50 MHz to 100 MHz, so it is possible for a device to be tested at or near the normal clock frequency.

Physical Basis of the Measurement

Semiconductors are characterized by a band structure with a nearly full valance band and a nearly empty conduction band. We build devices by modulating the number of charge carriers in these bands. This modulation affects not only the electronic properties but also the optical properties of the semiconductor. The particular optical property we are interested in is the index of refraction. An excess of free carriers ΔN causes a change in the index of n:

$$\Delta n = n\,\Delta N\, e^2 \Big/ \left(2\,\varepsilon\,\omega^2 m^*\right), \tag{1}$$

where e is the electronic charge, m^* is the effective mass of the carriers, ε is the dielectric constant, and ω is the angular frequency of the incident radiation.[4] Using numbers for silicon and 1-μm radiation we get

$$\Delta n \sim 10^{-21}\ \text{cm}^{-3} \Delta N\,. \tag{2}$$

A submicron FET can have an excess free-carrier concentration of 10^{20} to 10^{18} cm^{-3} extending to a depth l of 0.25 μm into the bulk.[5] A light pulse passing through this region (double pass) will experience a change in optical path ($l\,\Delta n$) of 0.0005 to 0.05 waves. The former value is probably beyond the resolution of our system, but 1/20 wave should be observable.

Free carriers are not the only contributors to the change in the index of refraction: temperature can also change the index of refraction. Typically the index of refraction will change by one part in 10^{-4} to 10^{-5} for each degree Kelvin.[3] The temperature can change because as current flows in the semiconductor, I^2R heating occurs. Two situations can develop: If the device is embedded in a silicon substrate, the high thermal conductivity will diffuse the energy over a large volume. Thus temperature rises of a few degrees can be distributed over as much as 500 μm, which is the typical substrate thickness. The small change in the index of refraction will be offset by the large path length. These combine to induce changes in the optical path lengths of about 1/20 wave. Alternatively, a buried SiO_2 layer can insulate the device from the substrate leading to 100°C temperature changes over a few wavelengths, again producing few-percent changes in the optical path length.[6] We estimate that the resolution of our imaging system is 0.02 waves limited by our 8-bit CID camera. This is based on an analysis of standard deviation of several identical measurements. This magnitude of change is easily seen in the silicon FET circuits we have examined.

We did not have a sufficiently detailed description of the device structure to calculate the combined effects of all the physical phenomena in a real device. That calculation would require a 3-D map of all the dopant and barrier layers, a detailed knowledge of the index of refraction of each of these structures, and the dependencies on temperature and free-carrier concentration. In addition, a dynamic model that simulates device operation and converts the output into optical-index-of-refraction data is required. Rather than developing such a first-principles method of evaluating our data, we have chosen a simpler, more empirical approach. A set of transistors was placed in the interferometer and set to a number of different voltage states. An interferogram was acquired at each state, and the differences were compared to see if the different voltage states were resolvable. This same criteria would apply if this diagnostic were fielded in a manufacturing setting, i.e., it would be used to determine if a particular transistor was working but would probably not be used to determine, for example, the exact carrier density in the gate channel of an FET.

The Tyman–Green interferometer[7] (see Fig. 72.41), which is used to determine the index-of-refraction changes, allows the whole substrate to be examined at once since it works with a large, collimated input beam. The interferometer uses a short-pulsed laser instead of a cw beam, which allows us to take time-resolved "snap-shot" interferograms. The interferometer is constructed as follows: The beam from a pulsed Nd:YAG laser (120 ps) is up-collimated in a telescope to a diameter greater than the DUT. The laser passes through a compensated absorbing doublet, which converts the Gaussian spatial profile into a flat-top. This beam strikes a 50/50 beamsplitter. The DUT acts as a mirror in one of the two interferometer arms. The second arm is terminated in a flat mirror. Both beams then retrace their respective paths back to the beamsplitter, where they recombine, i.e., the electric fields add. The combined beam passes through a pinhole to eliminate stray reflections from optical surfaces and grating reflections from the circuit elements, then through imaging optics, and finally onto a charge-injection-device (CID), 512 × 512 camera where the interference pattern is detected.

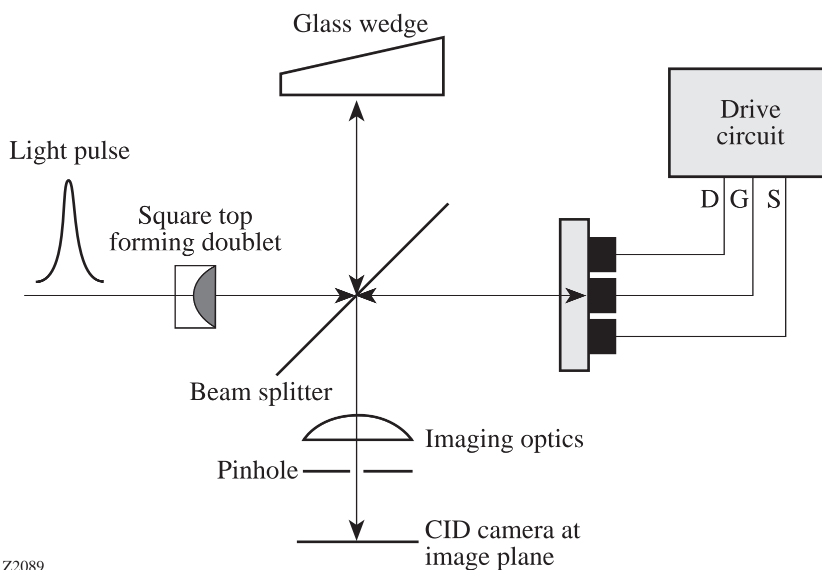

Figure 72.41
In the experimental setup a pulsed laser illuminates a Twyman–Green interferometer. The recombined beam was imaged onto a CID camera with 4-μm resolution.

The interferometer mixes the electric fields from the reference, E_{ref}, and device, E_{DUT}, arms to produce a total irradiance I. Due to differences in the optical path length the sum can be written as

$$E_{\text{ref}} + E_{\text{DUT}}\, e^{i\Psi}, \tag{3}$$

where Ψ is a phase angle. The detected quantity is actually the total irradiance obtained by multiplying the total electric field by its complex conjugate. We note that the intensity is equal to the square of the electric field times a constant, $I = \varepsilon c E^2/2$, where ε is the permittivity and c is the speed of light. Thus the total I irradiance can be written as[8]

$$I = I_{\text{ref}} + I_{\text{DUT}} + 2\left(I_{\text{ref}} I_{\text{DUT}}\right)^{1/2} \cos\Psi, \tag{4}$$

where I_{ref} is the reference-arm irradiance and I_{DUT} is the test-arm irradiance. The irradiance formula has three physically measurable quantities that are used to determine the phase angle Ψ, I_{ref}, I_{DUT}, and I. Several images must be acquired to accomplish this determination: First, I_{DUT} and I_{ref} are measured by alternatively blocking each of the two arms of the interferometer. Next, the interferogram I is acquired with both arms unblocked while the DUT is in a zero-voltage or inactive state. This enables the determination of $\Psi(\text{V} = 0)$. Finally, an image is acquired with the DUT in a known voltage state, which allows $\Psi(\text{V})$ to be determined. The interesting physical quantity is $\Delta\Psi = \Psi(0) - \Psi(\text{V})$ because it can be related to a length times a change in the index of refraction. The DUT may have different combination external voltages applied to it to determine $\Psi(\text{V})$ for different states.

Optics must be of high quality to make this device work; however, the most difficult optic to deal with is the DUT, which is typically a piece of silicon with semiconductor components fabricated on it. We want to probe the interior of this material, so the laser beam must penetrate the surface. The back surface of the device is the choice for the laser illumination because the interior structures are not obscured by surface metalization. However, the back surface of an IC is not typically optically polished and not parallel with respect to the front surface. Our test chips were polished but not parallel. Silicon has a 3.7 index of refraction, leading to a 32% reflection as the IR enters the material.[9] This reflection can combine with the interferogram and reduce the visibility of the fringes. The antiparallelism of the front and back surfaces produces beams that are not quite collinear. If the beams become sufficiently separated in the detector leg of the interferometer, a pinhole can be used to block the stray reflection. This pinhole must be selected carefully. If the pinhole is too small, it will attenuate the high spatial frequencies in the image, thereby reducing the resolution. The back side of the chip can be antireflection coated to minimize the reflection. We have demonstrated that an antireflection coating consisting of single quarter-wavelength-thick layer of HaO_2 can reduce the intensity of the reflection, but it is not clear that the device can survive the deposition processes.

The light source was a Nd:YAG laser operated at 30 Hz and was synchronized with the scan rate of our 512 × 512 CID camera. The laser pulse arrived during the blanking period of the frame to prevent extraneous noise in the image. The second mirror is the front surface of an uncoated glass wedge. The intensity of the reflection roughly approximated the average reflection from the DUT. From Eq. (4) it can be seen that the maximum fringe visibility will occur when the reference and test arms are exactly balanced. It was impossible to exactly balance the arms because the DUT is a nonuniform mirror. At some points the IR light will reflect off of surface metalization with a near-unity reflectivity; at other points it will encounter the bare silicon interface with 32% reflectivity; and at some points absorption in the IC will result in no reflected light.

Even with high-quality optics, it was impossible to completely eliminate large-scale fringes in our images due to multiple reflections and misalignment. The fringes were typically confined to a few well-defined frequencies. These were removed by Fourier transforming the image and filtering in the frequency domain.

A test structure provided by Intel consisted of several NMOS FET's with varying channel sizes. There was a common gate as well as a common source and P_{well} electrodes for all of the devices, but each device had a separate drain. The transistors were situated in a line between 100-μm-square drain contact pads with the source and gate being fed in through a bus line on either side of the pads. The back of the IC package was open to allow optical access to the back side of the chip. A circuit was constructed around each of the transistors consisting of a grounded source, a 2-V gate pulse supplied through a 3-MΩ resistor, and a variable-amplitude drain voltage supplied through a 500-kΩ resistor. For these tests, a 200-μs, 0- to 3-V pulse was applied to the common gate with and without the drain voltage present. Images taken under these conditions constitute the generalized set of images I_{DUT}. These images, together with the appropriate reference images, allow us to calculate the phase angles associated with each device state.

Experimental Results

The experimental results consist of the phase angles associated with each state of the transistors. Three different NMOS FET's were examined: a 1344-μm × 0.7-μm channel serpentine device, a 1.0-μm × 20-μm device, and 20-μm × 0.7-μm device. The first number represents the length of the source and drain electrodes; the second number is the width of the gate channel. Each device was illuminated in four different voltage states: no applied bias, gate bias only, drain bias only, and gate and drain together. The gate bias was pulsed for 100 μs, and the probe came in the middle of the pulse. The imaging of the device was such that each camera pixel corresponded to 4 μm × 4 μm; thus, several pixels were active for each device. The active pixels encompassed the gate channel, drain, and source regions. The phase angle presented for each state is the average over all of the active pixels. In addition several images were averaged to produce each measurement. The standard deviation of the value of Ψ as computed from the several images was always less than 1/30 wave and was typically less than 1/50 wave. Figures 72.42 and 72.43 show the phase variation for the three devices. The 1344/0.7 and the 1.0 μm × 20 μm show similar behavior with the phase angle increasing (with respect to the no bias case) as the gate is turned on, then decreasing as the drain is turned on. The last device shows different behavior, with the case of drain voltage without a gate being the most different of all the device states. However, without an underlying physical model it is impossible to interpret these results in terms of specific carrier-density changes. What is important is that the different states are resolvable. When transistors turn on, we see variations of 0.1 to 0.15 waves giving signal-to-noise ratios of from 3 to 5. A similar analysis on portions of the device containing no transistors found no correlation with applied voltage. This technique makes it possible to determine if a particular transistor in an IC is actually functioning.

Limitations to this technique are obvious: For example, there was also a 1.0/0.7-μm device on the Intel chip. Given our imaging system, this device should only have affected about

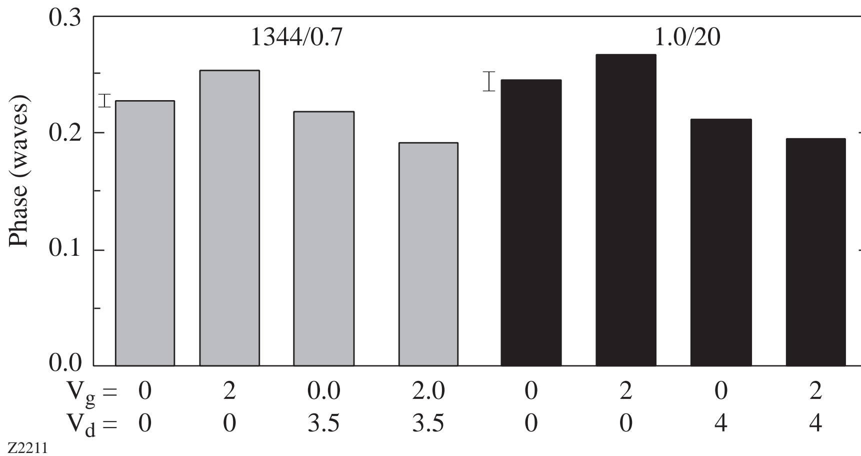

Figure 72.42
The 1344/0.7 and the 1.0-μm × 20-μm devices showed similar behavior. The error bars are displayed next to the 0 bias case.

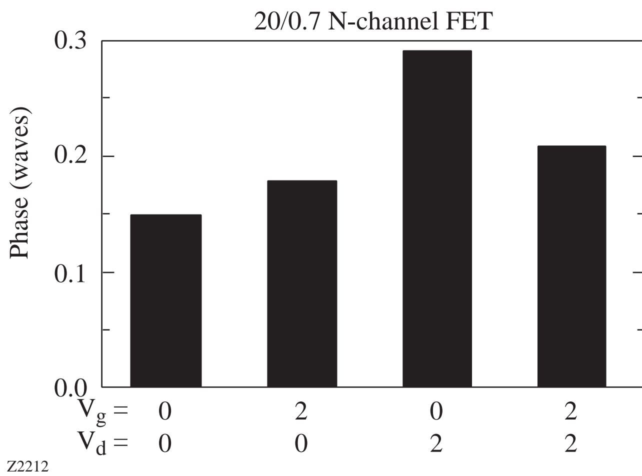

Figure 72.43
The 20/0.7 device showed the largest phase variations.

one pixel. We were unable to resolve this device. When we examined pixels likely to be associated with this device, no correlation was found with any applied voltages. Also, some structures on the IC precluded the use of this technique. Typically the metalized bonding pads showed up as dark spots on the IC images. This was unexpected since the metalization should have provided a good mirror. It is probable that the polysilicon used to electrically isolate the pad acts as infrared absorber. Thus another device located under a surface metalization structure was inaccessible because no light from that area reached the camera.

Conclusions

The technique described here offers an exciting new diagnostic for semiconductor integrated circuits. The technique is noninvasive and compatible with high-speed operation of integrated circuits. The picosecond time resolution enables us to either characterize specific logic states or even watch an individual device turn on. This imaging technique is sensitive to all of the index-of-refraction changes that can be associated with IC's, including heating due to current flowing through narrow wires and charge injection into the depletion region of a transistor. As more manufacturers shift to flip-chip technology and its associated inaccessibility of surface leads for device testing, the noninvasive nature of the interferometric imaging technique could enable it to become one of the few external IC testers still capable of operating with the latest chip designs. It should also be able to operate at the IC's rated clock speed.

The interferometric method examined and tested here will provide a very effective method of IC testing. The fringe sensitivity is of the order of 1/30 wave, which is sufficient to distinguish the voltage state of an FET in an integrated circuit. This work is in a preliminary state, and several improvements could easily be achieved by using an electronic camera with lower noise, using better optics with higher magnification, and applying antireflection coatings to reduce optical losses and eliminate stray beams. These improvements should make it possible to actually measure physical parameters such as the time-resolved carrier density in a switching transistor.

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