A Solid-State, Inductive-Adder, 10-kV Pulse Generator for Driving Large-Aperture Pockels Cells

Introduction

Pockels cells use electro-optic crystals with electrodes to apply electric fields that modulate the birefringence of the crystals and serve as voltage-controlled wave plates in laser systems. When combined with polarizers, these devices operate as optical switches for laser applications that include picking individual pulses from pulse trains, Q-switching laser cavities, isolating the gain of multiple amplifier stages, and protecting stages early in a power-amplifier chain from backward-propagating beams caused by unwanted retroreflections. These applications are illustrated schematically in Fig. 133.64. In this figure, a ring laser amplifier, such as the large-aperture ring amplifier (LARA)[1] or a similar system using Nd:YLF crystals for the laser gain (CLARA),[2] is shown.

Highly deuterated potassium dihydrogen phosphate (KD_2PO_4, often abbreviated KD*P or DKDP) is a common crystal used in Pockels cells, especially in devices that apply the electric field in the direction of the light beam propagation when large apertures are required. An important property of a Pockels cell is the half-wave voltage V_π. It is defined as the potential producing a retardance within the Pockels cell that rotates linear polarized light 90° to change the transmission state through an accompanying polarizer from minimum to maximum. The half-wave voltage for KD*P Pockels cells with longitudinal electrodes is approximately 8 kV, which is roughly independent of the aperture size. Voltage pulses up to 9 kV are needed to accommodate losses.

Figure 133.65 shows high-voltage pulse generation and delivery schemes used to drive Pockels cells. These cells form

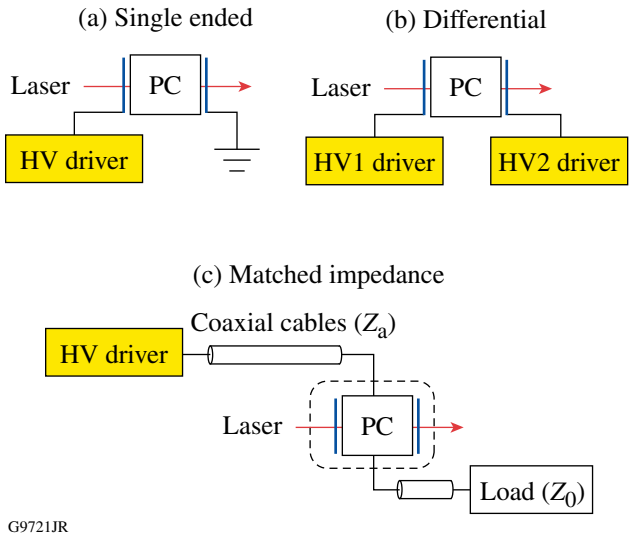

Figure 133.65
Pockels cell schemes. (a) A low-impedance, high-voltage (HV) half-wave driver is connected directly to the Pockels cell in the single-ended scheme. (b) Two low-impedance quarter-wave voltage drivers of opposite polarity are connected directly to the Pockels cell in the differential scheme. (c) In the matched-impedance scheme, a half-wave driver is connected to a Pockels cell, shunted with a resistance Z_0, via a coaxial line of characteristic impedance Z_0.

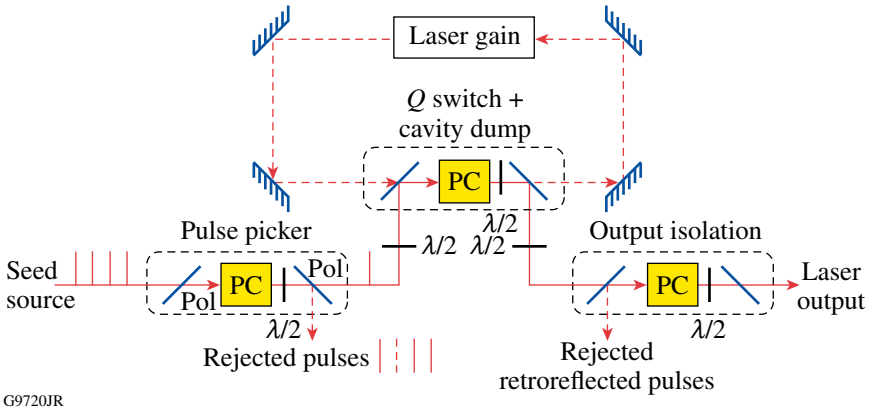

Figure 133.64
Applications of Pockels cells in laser systems. Pulse pickers use a Pockels cell (PC) between polarizers (Pol) in combination with a half-wave plate ($\lambda/2$) to select an individual pulse from a repetitive seed source. Output isolation stages similarly gate through single pulses to reject pulses leaked from multipass amplifiers; in addition, they protect front-end systems from retroreflected light. Pockels cells are used to Q-switch and cavity-dump multipass laser cavities.

capacitive loads with capacitance ranging from a few picofarads for small cells to hundreds of picofarads for large-aperture cells. Drive schemes include single-ended[3] [Fig. 133.65(a)] and differential[4] [Fig. 133.65(b)] schemes with short-length connections that directly drive the electrodes to limit pulse distortion resulting from parasitic reactances. Also illustrated is a matched-impedance driver[5] [Fig. 133.65(c)] that delivers high-voltage pulses on shielded coaxial cable to a resistively shunted Pockels cell with resistance equal to the characteristic impedance of the coaxial line Z_0. Two advantages of the coaxial-cable matched-impedance driver scheme are limited radiated electromagnetic interference (EMI) and the option of physical separation of the pulse generator from the Pockels cell with minimal distortion of the driver pulse shape.

A commonly used matched-impedance Pockels cell driver employs a thyratron electron tube as a closing switch to connect a fixed-length charged transmission line (charge line) to the Pockels cell.[5] This design generates high-voltage pulses with nanosecond switching times required for many applications. The charge line produces a rectangular pulse at half of the line charge voltage and twice the transmission line's pulse propagation length. Thyratrons designed for this application can switch voltages and currents up to 25 kV and 1 kA, respectively, and one device per pulser is generally used. Unfortunately, these electron tubes degrade with operation. Currently, aging thyratron pulsers are no longer serviceable since manufacturers have discontinued production of suitable thyratron replacement tubes.

It is desirable to replace thyratron-based drivers with drivers based on solid-state devices to avoid matched-impedance drivers based on modern solid-state devices is desirable to avoid degradation over time, improve reliability, and address availability issues associated with electron tubes. Several fast-switching, high-voltage, high-current technologies exist including metal-oxide-semiconductor field-effect transistors (MOSFET's),[6] avalanche bipolar transistors,[7] dynistors,[8] and drift-step-recovery diodes.[9] A fundamental advantage of MOSFET's compared to the other devices is that they can be turned on and off using low-voltage gate drive signals, allowing them to act as both opening and closing switches, making it possible to adjust output-pulse lengths without changing charge-line hardware. Avalanche and dynistor devices act only as closing switches and require a hardware pulse-forming network, such as a charge line, to set the duration of the output pulse. High-voltage MOSFET's are economical and produce fast switching speeds of less than 5 ns. Fast-switching, high-voltage MOSFET's can switch 1.2 kV at currents in the tens of amperes for each device and can be configured in various series- and parallel-connected networks to increase the total switching voltage and current capability.

The circuit topology used in this design—an inductive adder schematically illustrated in Fig. 133.66—is a circuit utilizing inductive coupling to achieve high-voltage pulse outputs from lower-voltage, ground-referenced pulse generators, or primary drivers. The output pulse is initiated when the switches in each primary driver simultaneously close and provide a current path from the charge-storage capacitors across the transformer's primary winding. The desired output level is obtained by series connecting, or adding, a sufficient number of individual transformer secondary windings. The pulse is terminated when the primary switches open and the primary current flow ceases. The lower-voltage primary driver units improve reliability and reduce switching device and charge-storage voltage requirements, as well as circuit layout stand-off requirements. The inductive-adder topology allows one to adjust both pulse amplitude and duration without changing the pulser's internal components.

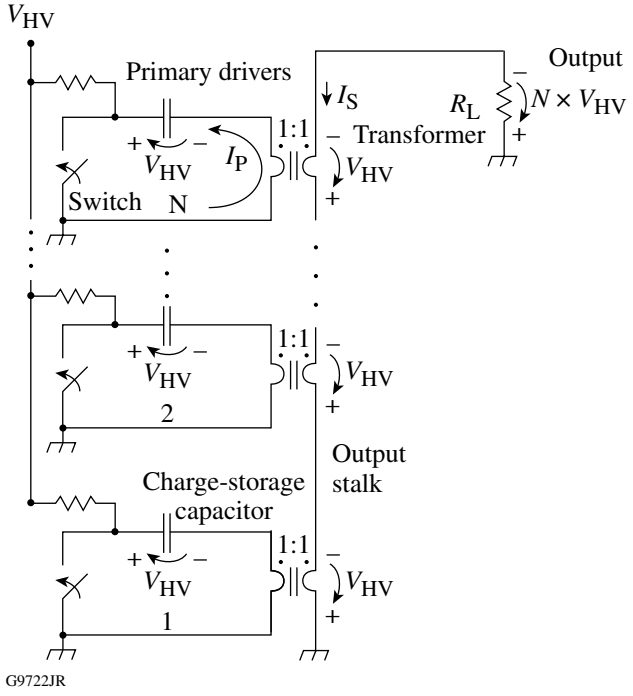

Figure 133.66
Inductive-adder schematic. When the switches simultaneously close within the N primary driver circuits, the charge-storage capacitance creates a current in the primary circuit of each coupled inductor (transformer). This current is inductively coupled to each transformer secondary and creates a voltage equal to the capacitor charge voltage. The secondary of each transformer is series connected to add the pulse voltage from each primary circuit and apply it to the load R_L.

Inductive-adder technology for driving Pockels cells has been demonstrated at voltages of tens of kilovolts and currents of hundreds of amperes with switching times less than 10 ns. Original designs were developed at Lawrence Livermore National Laboratory (LLNL) for fast pulse beam "kickers" in particle accelerators[10] and adapted at LLE to produce 20-kV pulses to switch the plasma-electrode Pockels cell (PEPC) in the OMEGA EP laser, where a closing and opening switch was required to produce the necessary double-pulse waveform.[11] Five solid-state switch-pulse PEPC driver (SS-SPD) units have been fielded at LLE since 2005 with performance and reliability far exceeding that of equivalent thyratron-based drivers.

A solid-state, high-voltage pulse generator based on inductive-adder technology for driving 50-Ω, KD*P Pockels cells is reported. The design considerations, subsystem characteristics, and electrical and optical performance are presented, as well as considerations to optimize the design for other potential applications.

Solid-State Pockels-Cell Driver Design

The requirements for a matched-impedance, solid-state Pockels-cell driver (SSPD) are summarized in Table 133.X. The output voltage and output impedance specifications determine the transmission values and stability for large-aperture KD*P Pockels cells[12] used in the half-wave applications illustrated in Fig. 133.64. The electrical pulse-timing values determine the maximum usable laser pulse length in a multipass laser amplifier and the maximum repetition rate of laser pulse trains from which a single pulse can be isolated.

Table 133.X: Solid-state Pockels-cell driver requirements.

Specification	Requirement
Output Voltage	
Peak output	5 to 10 kV
Peak voltage stability	<±3%
Pre-/post-pulse voltage	<±3%
Flattop variation	<±4%
Output Impedance	50 Ω
Pulse Timing	
10% to 90% rise time	<10 ns
90% to 10% fall time	<10 ns
Pulse duration	9 to 100 ns
Pulse jitter	<200-ps rms
Maximum repetition rate	10 Hz
External Trigger	5-V Logic Edge
Output Voltage Monitor	10,000:1
Primary Power	110/220 VAC, 50/60 Hz

State-of-the-art, fast-switching, high-voltage (1200-V) power MOSFET's, de-rated to 750 V, are utilized in the design of the primary drivers. A charge-storage voltage of 750 V requires an inductive-adder stack of at least 15 transformers to produce output-pulse voltages up to 10 kV, accounting for inductive coupling and driver losses. This circuit is shown schematically in Fig. 133.67. The 15 identical transformers and corresponding primary drive circuits are easily maintained, repaired, and inventoried as spares. An adjustable 750-V (dc) power supply charges all of the primary drive circuit charge-storage capacitors to the appropriate voltage for the desired pulse amplitude. The driver circuits are triggered simultaneously from a common trigger conditioning system initiated from an external 5-V logic trigger edge. Details of these subsystems and other features of the SSPD are provided below.

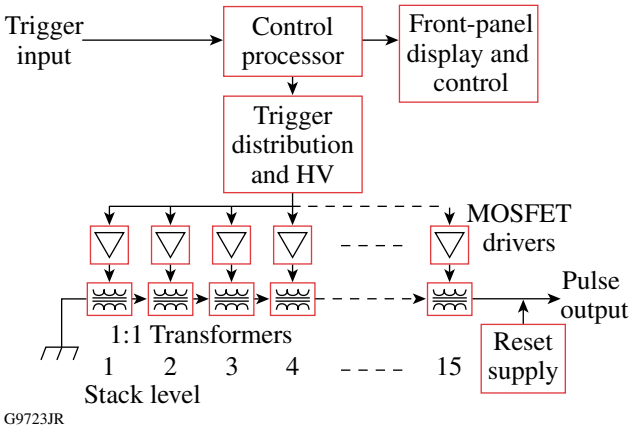

Figure 133.67
Schematic diagram of the solid-state Pockels-cell driver (SSPD). The pulser consists of 15 ground-referenced drivers, each driving a 1:1 transformer with secondaries series-connected to form the high-voltage output pulse.

1. Pulse Transformer Design

An inductive-adder transformer is illustrated in Fig. 133.68. The transformer uses a single-turn, solid primary winding machined from aluminum that completely surrounds a toroidal transformer core [Fig. 133.68(a)]. This configuration maximizes the inductive coupling between primary and secondary by minimizing the leakage inductance from uncoupled magnetic fields. Leakage inductance appears in series with the primary drive circuit, directly impacting high-frequency performance and resulting in increased pulse transition times and reduced pulse amplitude. The secondary circuit of the transformer

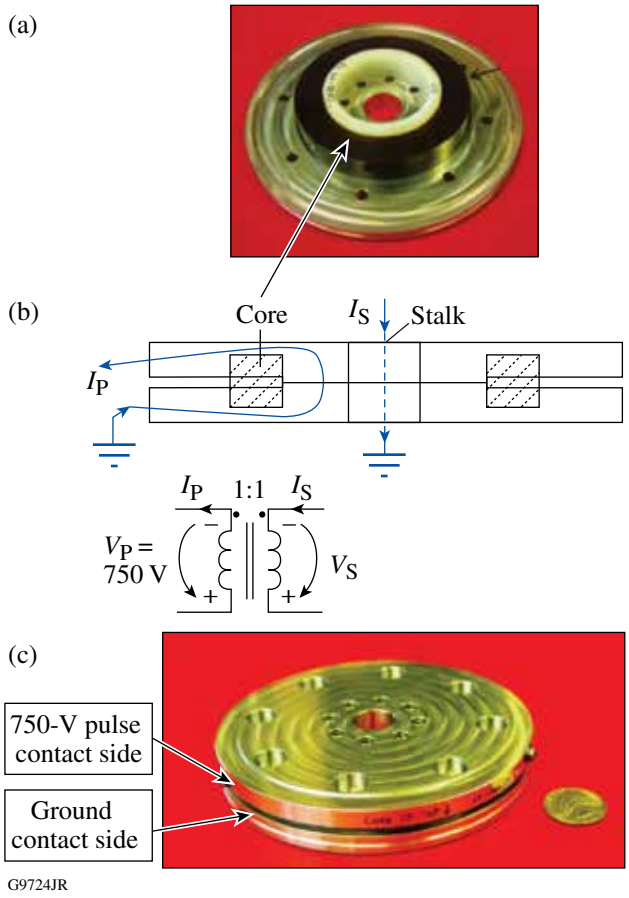

Figure 133.68
Inductive-adder transformer cell. [(a),(b)] The 750-V pulse contact side of the primary winding of a cell is isolated from the ground side of the next transformer above by standoffs seated on the ground contact side. (c) The standoffs are positioned in eight cut-outs (holes) in the 750-V side with sufficient air-gap clearance. The standoffs provide both isolation of the 750-V contact side and connection of successive transformers ground contact sides in the stack. Threaded rods extend through the center of the standoffs to hold the cells in the stack together. An isolated conductive rod extends through the center hole of each transformer to form the series-connected secondary circuit.

structure is created by passing an isolated metal rod through the center of the transformer structure [Fig. 133.68(b)]. This metal rod extends through the entire stack of transformer cores, thereby series-connecting the secondaries of each. This rod is termed the "stalk."

A toroid core geometry was chosen to create an efficient magnetic coupling path between the primary and secondary that had minimal leakage inductance. The size of the core is selected to have sufficient cross-sectional area and magnetic path length (average circumference) to support the pulse voltage–time product without magnetic-flux saturation of the core material. If core flux saturation occurs, the single-turn primary drops to a very low impedance, which results in catastrophic over-current failure of the primary drive circuits. A safety margin was applied to the design of the transformer core to ensure that the magnetic-flux density in the core is three times less than the saturation flux density for the longest pulse of the largest amplitude.

The first step in the design is to determine the core material and size for the 1:1 single-turn transformer. The core is constructed from a tape-wound, low-loss amorphous ferromagnetic alloy. The core material was selected for its large saturation flux density and low loss. This type of core provides high coupling over a wide bandwidth extending into the VHF (very high frequency) range. The core material chosen was Metglas 2601SA1 (Ref. 13), which is the same material used in the SS-SPD for the OMEGA EP PEPC pulser.[11] The material saturation flux density swing (ΔB_{sat}) is 3 teslas (T). The maximum operational flux density was set at 1 T to provide a 3× safety margin. The core effective cross-sectional area A_e to achieve this flux density is derived from the standard equations for flux density B (tesla), inductance L (henrys), and voltage of a toroid wound inductor:[14]

$$A_e = \frac{3 \cdot V \cdot \Delta t}{\Delta B_{sat} \cdot PF} \left(\mathrm{m}^2\right), \tag{1}$$

where V is the maximum voltage across the primary circuit for the pulse duration Δt and PF is the core packing factor defined as the ratio of the ferromagnetic material cross-sectional area to the overall cross-sectional area of the core material. The value of 3 in the numerator relates to the safety margin.

With the values of V = 750 V, Δt = 100 ns, ΔB_{sat} = 1 T, and PF = 0.65, A_e = 1.15 cm^2 is obtained. A toroid core with a 1.27-cm^2 cross section was chosen. Once the cross-sectional area is calculated, the circumference of the toroid must be determined. For a transformer, the inductance of a winding, with all others open-circuited, is termed the "magnetizing inductance." This inductance is electrically in shunt with the drive or load circuitry of that winding. The magnetizing inductance must be large enough that the current through the inductor at the end of the maximum amplitude pulse will not create distortion by excessive loading. Ideally, a large inductance is desirable; however, a tradeoff must be made since a large inductance requires a small core diameter. A small core diameter decreases the driver circuit board's component placement area if minimum current path length is required for low leakage inductance. The circumference was selected

as a compromise between magnetizing inductance value and driver circuit board's component physical layout. The chosen 3-in. outer diameter produces a magnetizing inductance of approximately 2 μH as calculated using Eq. (2) (Ref. 14):

$$L = \frac{\mu_0 \mu_r N^2 A_e}{l_e} (\mathrm{H}), \tag{2}$$

where the number of turns $N = 1$, $\mu_0\mu_r$ is the core material's magnetic permeability, and the effective magnetic path length or the average circumference l_e is $2\pi(r = 2.5\text{-in.}/2)$. An inductance of 2 μH produces a magnetizing current of about 13% of the total primary current at the end of the longest pulse operation.

Another characteristic of the ferromagnetic core material is the core magnetization current. This current is required to overcome the permanent magnetization of the core material since it will take on an amount of permanent magnetization. This is exhibited in the hysteresis loop of the B–H curves (magnetic field versus flux density).[13] An ~45-A magnetization current is required for the core material chosen in this design to overcome the magnetization hysteresis.

2. Primary Drive Circuit

A simplified schematic of the transformer and the associated primary drive circuit is illustrated in Fig. 133.69. The primary drive to each transformer of the inductive adder is produced by a low-impedance, pulsed-voltage source formed by a group of 12 parallel-connected MOSFET's and a bank of charge-storage capacitors. The pulsed-drive units are connected to the primary winding along its circumference to minimize parasitic inductance. The primary driver is split into two identical printed wiring boards that plug into the transformer circumference from opposite sides for ease of assembly and maintenance. The number of parallel-connected MOSFET's for each primary driver is determined by the sum of the current required at the output plus the core magnetizing and magnetization currents. The total primary current is equally divided among the parallel-connected, synchronously triggered MOSFET's. The design uses a higher MOSFET count than what is minimally required to switch the output current level to provide a safety margin. In the SSPD design, the maximum MOSFET operational current is limited to 64% of the MOSFET pulsed maximum current as specified by the MOSFET manufacturer.[6]

The primary-driver board is illustrated in Fig. 133.70. This board contains the high-voltage-power MOSFET's as well as the MOSFET gate-driver integrated circuits and charge-storage capacitors. The MOSFET gate-driver integrated circuit is a low-voltage (24-V), 14-A peak switching current driver specifically designed to drive MOSFET gates with nanosecond switching times. Each MOSFET has its own gate driver to maximize switching speeds. The charge-storage capacitors charge to the potential of the primary pulse voltage, which is theoretically 15× less than the actual output-pulse voltage. The capacitors are effectively connected across the primary winding when the MOSFET turns on (low impedance from drain to source). The pulse output current flows from the discharging storage capacitors through the primary winding and is coupled to the secondary via the transformer. The charge-storage capacitor value is calculated to support the output current pulse requirement with less than a 1% droop in charge voltage over the maximum

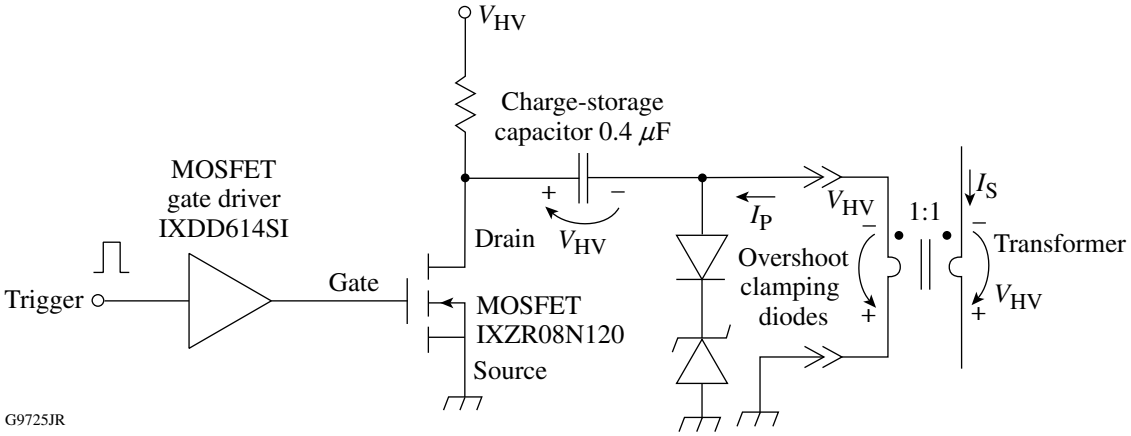

Figure 133.69
Schematic of the transformer primary drive circuit.

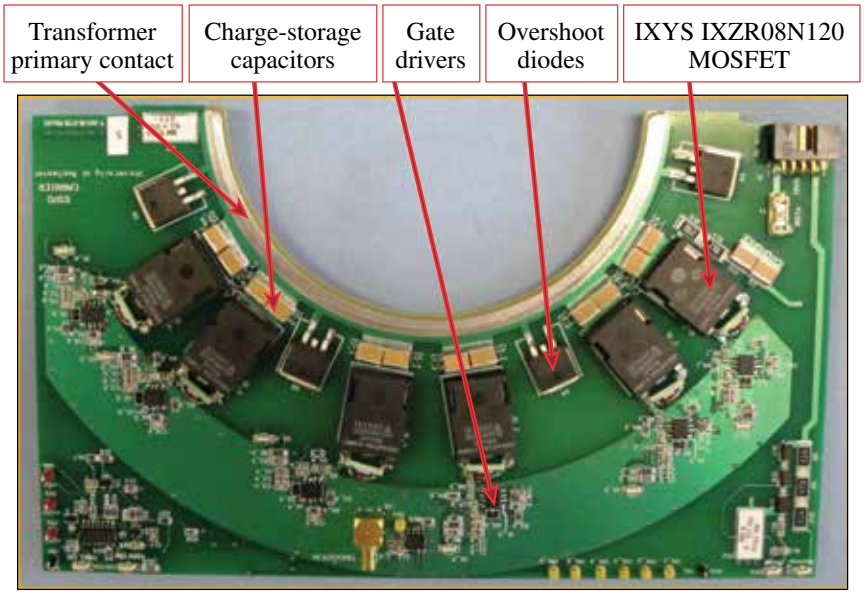

Figure 133.70
MOSFET driver board. The MOSFET driver board contains the circuitry to produce the pulsed voltage to the primary of the inductive-adder transformers. Each transformer has two driver boards that plug in and connect to the circumference of the primary winding. Each driver board contains six MOSFET's.

pulse duration. Overshoot clamping diodes are included in the driver circuit and connected across the transformer primary. The diodes clamp the inductive spike voltage produced by the magnetizing and leakage inductance when the MOSFET driver turns off (high impedance from drain to source). Clamping prevents the drain-to-source spike from exceeding the breakdown voltage of the MOSFET's while preventing output post-pulse ringing and overshoot.

To drive the 50-Ω–loaded LARA and CLARA Pockels cells, the maximum load current is 200 A with the maximum load voltage set at 10 kV. The total primary current is approximately 280 A, including the magnetization current and the magnetizing inductance current. IXYS-Colorado Semiconductor IXZR08N120 1200-V MOSFET's were chosen to provide sufficient voltage-breakdown headroom to prevent inductively generated overshoot in the transformer primary circuit waveforms from damaging them. These devices are also designed for ultralow internal capacitance and parasitic inductance to enhance switching speed. Twelve MOSFET devices are connected in parallel for each primary winding to limit the drain switching current to 23 A per device for the maximum duration and amplitude output pulse. The MOSFET pulsed drain current rating is significantly higher (40 A) (Ref. 6), but allowances are made for adverse load conditions, such as capacitive transients and arc-over short circuits.

When switching a MOSFET, the gate is biased positively with respect to the source to create a negative charge accumulation within the drain-source conduction layer. The gate is insulated from the other terminals of the device by the gate oxide layer above the conduction channel. The negative charge in the conduction layer creates a low-impedance channel for electron flow between the drain and source, thereby turning the MOSFET switch on. The insulated gate is mainly capacitive in nature with respect to the other terminals of the device. The gate capacitance is increased by the Miller switching capacitance effect between the gate and drain while they are changing potential.[15] Taking the Miller effect into account, the total gate input switching capacitance is of the order of 28 nF. The MOSFET gate driver's integrated circuit (IC) from the Clare Semiconductor division of IXYS (IXDD614SI) provides peak gate currents up to 14 A to charge and discharge the gate input switching capacitance. With 14 A, the charge rate for 28 nF across the gate switching transition of 2.5 V is 4.9 ns. This rate is fast enough to switch the MOSFET in the time required by the overall pulser performance specification.

The charge storage for the primary current pulse must be sufficient to restrict voltage droop over the pulse duration. For the SSPD design, the droop was limited to 7.5 V (1%) for a 100-ns pulse at full load current. The total charge-storage capacitance was calculated to be 4.8 μF to meet this require-

ment. This is divided into 12 0.4-μF capacitor blocks, one in the drain circuit of each of the 12 MOSFET's. Each capacitor block is formed from four individual 0.1-μF, 1000-V ceramic multilayer capacitors.

Groups of overshoot clamping diodes are connected across the primary transformer winding to dissipate the energy within the leakage and magnetizing inductance after the MOSFET's are turned off. This limits ringing and overshoot on the trailing edge of the output pulse and protects the MOSFETs from overvoltage breakdown failure.

The charge storage, MOSFET's, and driver IC's are split into two boards that plug into the circumference of the transformer primary winding to minimize circuit path lengths, thereby minimizing the leakage inductance effects. Splitting the drivers onto two boards also simplifies transformer assembly and removal/repair of the driver boards. Each board contains diagnostic test points and light-emitting–diode (LED) fault indicators to facilitate diagnosis of board failures. Diagnostics are focused on isolating failures down to the component level for quick repair turnaround.

Fifteen identical driver/transformer units (30 driver boards and 15 transformers) are required in the pulser stack to sum the output level to that required in the output specifications defined in Table 133.X. The inductive-adder stack is illustrated in Fig. 133.71.

3. Output Stalk

The series-connected secondary of the stacked transformers is a single conductive rod (the output stalk) that extends through the center of each transformer. One end is connected to ground and the other is connected to the 50-Ω output connector. Previous modeling studies have indicated that the stalk characteristic impedance should be set equal to the standard load impedance for optimal rise- and fall-time performance.[16] The stalk characteristic impedance is given by

$$Z_0 = \sqrt{\frac{L_{\text{stalk}} + L_{\text{leakage}}}{C_{\text{stalk}}}}, \tag{3}$$

where L_{stalk} is the inductance of the stalk per unit transformer length, L_{leakage} is the transformer leakage inductance for each individual transformer placed in series with the stalk inductance with the MOSFET switch on, and C_{stalk} is the capacitance of the stalk to ground per unit transformer length. For this design, the stalk diameter is adjusted to provide optimal matching to 50 Ω, the load impedance of the pulser.

4. Control

Overall control of the pulser is accomplished by utilizing an embedded microprocessor. The microprocessor controls operational conditions of the pulser and monitors safety and failure detection circuits. The processor is capable of remote control communications via an Ethernet connection; however,

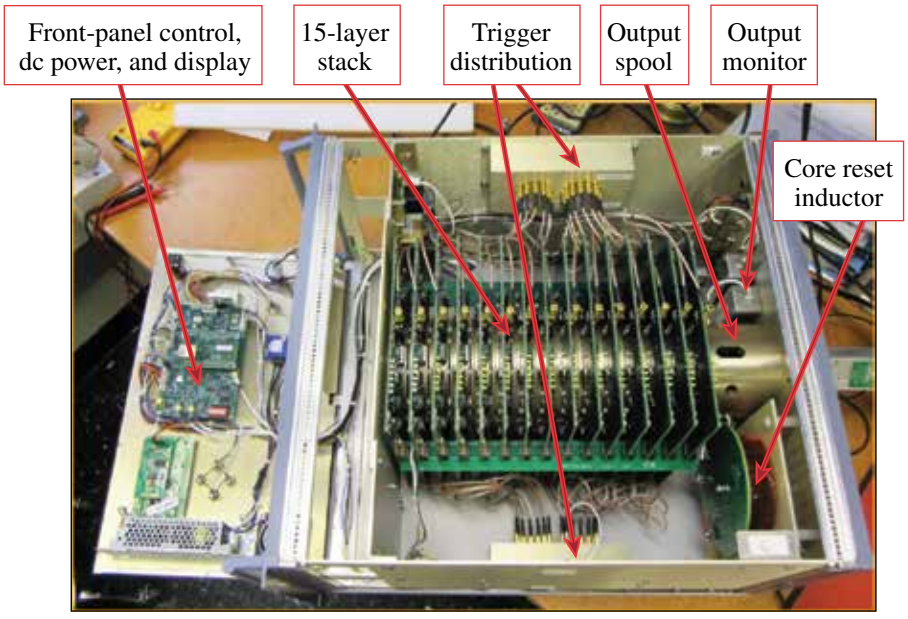

Figure 133.71
SSPD pulser stack with top cover removed and front panel open. All circuit boards are accessible without major disassembly of the enclosure.

this feature has not been implemented in the current design pending an operational need. The control assembly also conditions the incoming trigger to produce the desired output-pulse length. The externally supplied input trigger pulse edge is used to initiate an adjustable-width pulse generator, which is the source for internal synchronous triggers utilized by each of the 30 driver boards. The pulse length is adjustable in binary steps with a maximum length of 100 ns and a resolution of 0.5 ns. The front-panel interface is also implemented within the control assembly. This interface provides a menu-driven display with a simple push button panel for control of the pulser operation.

5. Front-Panel Display

The front-panel display is an LCD-backlit display that provides pulser operational information. The display includes three pages of information containing control firmware revision status, pulse voltage setting and output level, pulse output length, pulse output state (on/off), and fault status.

6. Trigger Distribution

Each of the 30 driver boards requires a synchronous trigger of the appropriate duration for the desired output pulse. To accommodate this, we use two 1-to-15 active trigger splitters whose trigger source is supplied by the trigger conditioning circuits on the control assembly board. Each splitter has a trigger driver integrated circuit and a resistive trigger splitter that can drive 15 driver board trigger inputs terminated in 50 Ω. The triggers are supplied to each transformer driver board via equal-length, 50-Ω shielded coaxial cables to maintain synchronization of all triggers on the stack.

7. Reset-Current Circuit

The output pulse is a unipolar pulse, and over repeated pulses, the transformer cores will take on a permanent magnetization that will saturate the magnetic core material. To avoid core saturation, a direct current (dc) is connected into the output stalk of opposite polarity to the output current. The dc current is called the "core reset current." The supply to produce this current must be isolated from the output pulse with a low-pass filter constructed from a large series inductor capable of withstanding the longest-duration and maximum-amplitude pulse output voltage.

8. High-Voltage Power Supply Control

The high-voltage supply is the main charging supply for the charge-storage capacitors on the MOSFET primary circuit driver boards. This supply is adjustable from 0 to 750 V in accordance with the desired output-pulse voltage. This supply is set by the controller board in response to an operator's front-panel commands. The controller board monitors a scaled version of the supply output voltage to verify that the supply is operating correctly. The controller displays the monitor value as well as the set-point value on the front-panel display.

9. Housekeeping Supply

The low-potential dc power for all of the circuit boards throughout the pulser is provided by the housekeeping power supply, which is 24 V dc. Lower voltages, like 12 V, 5 V, and 3.3 V, are regulated down on individual boards as required by the circuitry contained on each assembly. The controller board monitors the 24-V housekeeping supply and will issue a fault if the supply drops below a prescribed fault threshold value.

10. Enclosure

The packaged SSPD prototype is shown in Fig. 133.72. The enclosure is a standard 19-in. rack-mount chassis that is six rack units (6 U = 10.5 in.) high and 20 in. deep. The enclosure is designed to facilitate assembly and for ease of pulser repair. All stack MOSFET driver boards are accessible through removable top and bottom covers, as shown in Fig. 133.71. The front panel hinges forward to allow access to the control board and dc supplies.

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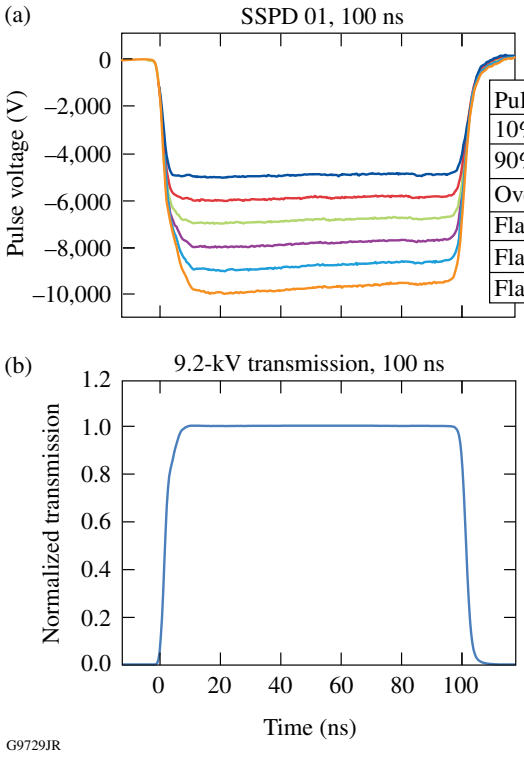
Figure 133.72
Solid-state Pockels-cell driver package.

11. SSPD Electrical Performance

Two SSPD prototype units were assembled and tested with nearly identical performance into a 50-Ω load network. Figure 133.73(a) illustrates electrical output for approximately 100-ns-long pulses at various output levels. The inset table summarizes the performance parameters at the approximate quarter- and half-wave voltages for KD*P Pockels cells (5 kV and 10 kV, respectively). Figure 133.73(b) shows the measured



Pulse amplitude	5.0	10.0	kV
10% to 90% rise time	4.8	8.8	ns
90% to 10% fall time	9.6	12.8	ns
Overshoot	6.0	2.3	%
Flattop maximum	–2.1	–2.6	%
Flattop minimum	2.9	3.0	%
Flattop width	93.6	86.0	ns

Figure 133.73
(a) Measured 100-ns output pulse electrical waveforms and (b) 100-ns measured Pockels-cell system transmission for Cleveland Crystals TX5065 (Ref. 12).

transmission of a Pockels cell [Cleveland Crystals TX5065 (Ref. 12)] driven by the SSPD. Similarly, Fig. 133.74 shows the measured electrical SSPD output and calculated optical performance for approximately 25-ns pulses.

A prototype SSPD pulser was connected to a 25-mm Pockels cell [Cleveland Crystals TX-2650 (Ref. 12)] operating as a cavity *Q*-switch in a CLARA and tested. Measured laser performance, including energy stability and pulse shape, matched performance produced by the thyratron pulser that was replaced by the prototype SSPD unit.

Future Considerations

Future enhancements can be explored to improve SSPD operation, including optimizing the transformer core size to improve output-pulse fidelity. Core selection can be further optimized to improve rise and fall time as well as reduce the magnetization current. The mechanical design of the transformer can also be improved to reduce the cost of manufacture as well as weight.

The number of parallel-connected MOSFET's in each stack could be reduced by working each at higher pulsed currents. This may improve switching speed and reduce the driver size but may reduce the overcurrent safety margin. The same may be accomplished as future higher-performance MOSFET devices are developed without impacting safety margin. Overall, a reduction in MOSFET count could reduce the total parts count and size of each driver board with potential reductions in the overall size and weight of the pulser enclosure.

As noted in Fig. 133.74, the trailing edge of the two largest-amplitude, 25-ns pulses has a tail that increases the rise time. Future work may expose the cause of this and determine a correction.

Summary

A solid-state, 50-Ω, 10-kV, 100-ns Pockels-cell driver has been designed and assembled as a replacement for aging thyratron switched drivers. The design is based on the inductive-adder approach developed at Lawrence Livermore National Laboratory. Performance tests in a CLARA produced results equivalent to the thyratron driver in the same application.

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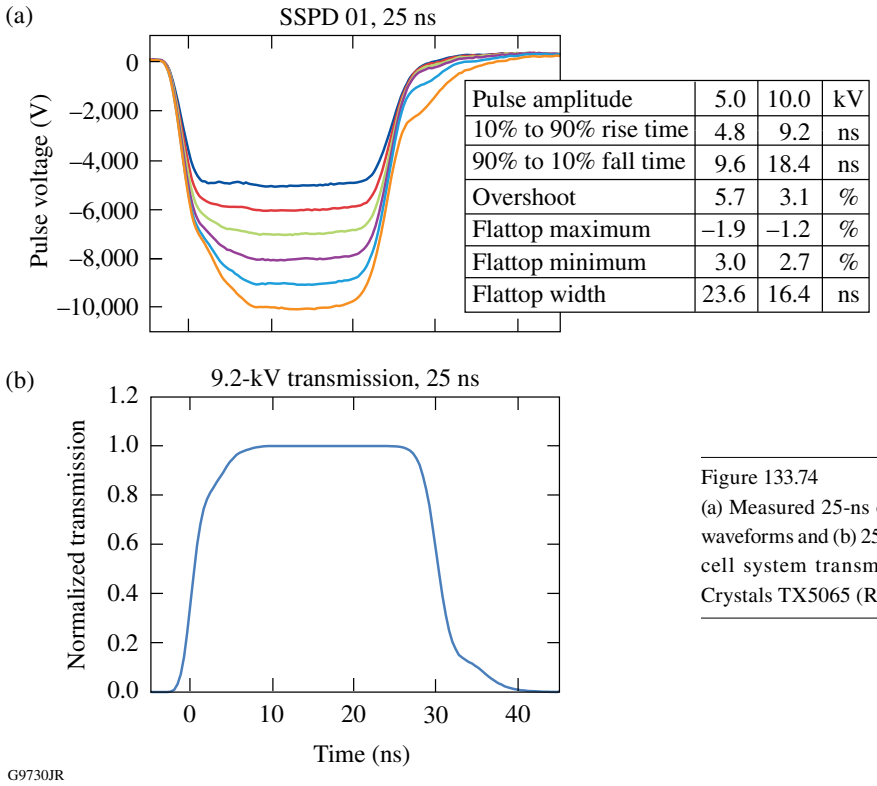

Pulse amplitude	5.0	10.0	kV
10% to 90% rise time	4.8	9.2	ns
90% to 10% fall time	9.6	18.4	ns
Overshoot	5.7	3.1	%
Flattop maximum	–1.9	–1.2	%
Flattop minimum	3.0	2.7	%
Flattop width	23.6	16.4	ns

Figure 133.74
(a) Measured 25-ns output pulse electrical waveforms and (b) 25-ns measured Pockels-cell system transmission for Cleveland Crystals TX5065 (Ref. 12).

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