Ultra-Wideband Pulse Generation, Detection and Filtering Using Distributed Architectures and Circuit Techniques

by

Yunliang Zhu

Submitted in Partial Fulfillment of the Requirements for the Degree Doctor of Philosophy

Supervised by
Professor Hui Wu

Department of Electrical and Computer Engineering School of Engineering and Applied Sciences The College

University of Rochester Rochester, New York

2008
Curriculum Vitae

Yunliang Zhu was born in Nanjing, China on September 20, 1981. He attended Nanjing University from 1999 to 2003, and graduated with a Bachelor of Science degree in 2003. He came to the University of Rochester in the Fall of 2003 and began graduate studies in Electrical Engineering. He pursued his research in RF/microwave integrated circuits under the direction of Professor Hui Wu and received the Master of Science degree from University of Rochester in 2004. He received the first Robert Mundell Fellowship at Nanjing University in 2002 and Frank J. Horton Research Fellowship at University of Rochester from 2004 to 2008. He was the Best Student Paper winner (1st place) at 2008 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF).
Acknowledgment

I take this opportunity to express my profound gratitude and deep regard to my advisor, Professor Hui Wu, for his exemplary guidance, stimulating suggestions and constant encouragement through the course of this PhD work. During last five years, he has always inspired me with his full enthusiasm for scientific discoveries and technical innovations, enlightened me with his fascinating insights in every subject, and help me with his extensive hands-on experience in experiments. I am also deeply indebted to him for his kindness and friendship in these years.

Sincere appreciation is extended to Dr. Jonathan Zuegel and Dr. John Marcianc who have always been there to offer me directions and encouragement during the course of CAEPS Project. I thank Professor Wayne Knox, Professor Roman Sobolewski, Professor Azadeh Vosoughi and Professor Wendi Heinzelman for their invaluable time taken in my thesis defense and proposal exam. I thank Professor Gaurav Sharma and many other professors for the wonderful teaching of my course work.

I would like to express my gratitude to all members of Professor Wu’s research group, Jianyun Hu, Shang Wang, Lin Zhang, David Karasiewicz and Berkehan Ciftcioglu. I especially would like to thank my friends, Jie Zhang, Yan Zhang, Xiaoxu Liu, Emre Salman, Jonathan Rosenfeld, Vasilis Pavlidis, Yuxin Wang, Yunan Xiang, Quentin Diduck, Eric Moule, Allen Cross, John Liobe, Michael Wieckowski, Jingjing Zhang, Guoqing Chen, Bo Fu, Oktay Altun, and many others for their friendship.

I would like to acknowledge the U.S. Department of Energy Office of Inertial Confinement Fusion under Cooperative Agreement No. DE-FC52-92SF19460, the
University of Rochester, and the New York State Energy Research and Development Authority for financial support, and National Semiconductor for chip fabrication. I would like to thank Laboratory for Laser Energetics for the support of my PhD research through Frank J. Horton research fellowship. I would like to thank Bijoy Chatterjee, Ahmad Bahai, Peter Holloway, Mounir Bohsali, Johnny Yu, Anish Shah, Virginia Abellera, Peter Misich, and Jun Wan of National Semiconductor for their help and support in chip fabrication.

Finally, I would like to give my special thanks to my parents, whose patient love enabled me to complete this degree.
Abstract

The generation, detection and filtering of ultra-wideband (UWB) pulses have become increasingly important in wireless communications, fiber-optical communications and pulse radar systems. Wideband integrated circuits (ICs) in complementary metal oxide semiconductor (CMOS) technology are of particular interests for these applications due to the following advantages: low cost, large scale integration capabilities, and fast technology development. However, CMOS technologies also bring great challenges in designing wideband ICs. To overcome these challenges, circuit complexity can be traded for speed and power by operating multiple circuit blocks cooperatively, i.e., using distributed circuits. On the other hand, digital circuits can be integrated into radio frequency (RF) ICs to improve the performance, e.g., dynamic range. This dissertation presents our studies on UWB pulse processing using (a) distributed architectures and circuits, and (b) digitally-assisted RF techniques. Chip prototypes in 0.18µm standard digital CMOS technologies are demonstrated for the following UWB pulse processing circuits.

For UWB pulse filtering, we incorporated non-uniform filtering structures into distributed amplifiers (DAs) using the network synthesis method for spectrum control over both passband and stopband. Two DA prototypes with Butterworth and Chebyshev filtering were implemented. Filtering functions can also be implemented in DAs by combining multiple signals noncoherently, which leads to the development of distributed transversal filters (DTFs).

For UWB pulse generation, multiple pulse generators are time-interleaved in a distributed architecture with wideband pulse combining using an on-chip transmission line. This newly-developed circuit, distributed waveform generator (DWG) can

In a similar distributed architecture, multiple pulsed multipliers can be time-interleaved to detect UWB pulses. Such a distributed pulsed correlator (DPC) has the built-in template pulse generator and uses an on-chip transmission line for pulse distribution. A 10GS/s differential DPC prototype has been implemented as the RF front-end of an IR-UWB receiver, which achieves 40pJ/b with 250Mbps data rate.

To improve dynamic range using digitally-assisted RF techniques, digital-to-analog converters (DAC) assisted pulse generators were incorporated into a 10.9GS/s DWG prototype to achieve more than 20dB dynamic range of pulse generation. Similarly, binary-weighted gain cell was adopted in a DTF design for enhancing the dynamic range.
# Contents

Curriculum Vitae ii

Acknowledgment iii

Abstract v

List of Tables xi

List of Figures xii

1 Introduction 1

1.1 Performance Issues in Wireless Communications ............... 1

1.1.1 Bandwidth and Data Rate .................................... 2

1.1.2 Power Efficiency ............................................. 4

1.1.3 System Reconfigurability .................................... 4

1.2 Challenges in CMOS RF Integrated Circuits ............... 5

1.3 Applications of Ultra-Wideband Pulse Processing .............. 8

1.3.1 Impulse Radio UWB Communications .................... 8

1.3.2 Pulse Filtering in Laser Systems ....................... 13

1.4 Contributions of This Dissertation .......................... 14

1.5 Dissertation Organization ................................... 15

2 Conventional Wideband Circuit Techniques 17

2.1 Wideband Amplifier Design .................................... 18

2.1.1 Shunt-Peaked Amplifiers .................................... 18
2.1.2 Series-Peaked Amplifiers ........................................ 19
2.1.3 Shunt-Series Amplifiers .......................................... 20
2.1.4 $f_T$ Doubler .......................................................... 21
2.1.5 Capacitive Degeneration .......................................... 22
2.1.6 Cherry-Hopper Amplifiers ....................................... 23
2.1.7 Balanced Amplifiers ................................................ 24
2.2 Gain-Bandwidth Product Limit ...................................... 25
2.3 Distributed Circuits and Systems .................................... 26
  2.3.1 Distributed Amplifiers .......................................... 26
  2.3.2 Distributed Architectures ...................................... 29

3 Distributed Pulse Filtering Circuits .................................. 30
  3.1 Introduction ......................................................... 30
  3.2 Distributed Amplifiers with Non-Uniform Filtering Structures .... 32
    3.2.1 Non-Uniform Filtering ......................................... 35
    3.2.2 Circuit Design .................................................. 36
    3.2.3 Measurement Results ......................................... 38
  3.3 Distributed Transversal Filters ................................... 42
    3.3.1 DTF Architecture ............................................. 43
    3.3.2 Pulse Filtering Analysis ...................................... 45
    3.3.3 Circuit Level Transfer Functions of DTF .................... 46
    3.3.4 Noise Analysis ................................................ 49
    3.3.5 DTF Prototype for Pulse Filtering in Laser Systems ........ 50
    3.3.6 DTF prototype for Pulse Filtering in IR-UWB Systems ...... 57
    3.3.7 DTF Performance Limitations ................................ 67
  3.4 Summary ............................................................ 68

4 Distributed Waveform Generators .................................... 70
  4.1 Introduction ........................................................ 70
  4.2 Conventional UWB Pulse Generators ............................ 73
  4.3 DWG for UWB Pulse Generation ................................... 76
    4.3.1 UWB Pulse Characteristics .................................. 76
4.3.2 DWG Architecture ........................................ 78
4.3.3 Peak Sampling ............................................ 79
4.3.4 Built-in Pulse Shaping .................................... 81
4.3.5 Modulation Capabilities ................................. 83
4.3.6 Performance Limitations ................................. 85
4.4 Single-Polarity DWG Prototype .......................... 85
  4.4.1 Circuit Design ........................................... 85
  4.4.2 Measurement Results .................................... 89
4.5 Dual-Polarity DWG Prototype for IR-UWB Transmitter .. 94
  4.5.1 Circuit Design ........................................... 94
  4.5.2 Measurement Results .................................... 100
4.6 DAC-Assisted DWG with Current-Steering Pulse Generators .. 107
  4.6.1 Circuit Design ........................................... 107
  4.6.2 Measurement Results .................................... 110
4.7 DWG Based IR-UWB Transmitter with Pulse Shape Modulation .. 114
  4.7.1 Circuit Design ........................................... 114
  4.7.2 Measurement Results .................................... 117
4.8 Summary .................................................. 120

5 Distributed Pulsed Correlators .............................. 122
  5.1 Introduction ................................................ 122
  5.2 Distributed Pulsed Correlator Architecture .......... 125
  5.3 Differential DPC Prototype .............................. 126
    5.3.1 Circuit Design ........................................ 126
    5.3.2 Measurement Results ................................ 129
  5.4 Summary .................................................. 134

6 Wideband Directional Coupler in Digital CMOS Technology .... 135
  6.1 Introduction .............................................. 135
  6.2 Microwave Directional Coupler .......................... 136
  6.3 Broadside Coupled Directional Coupler Design .......... 138
  6.4 Measurement Results ...................................... 141
6.5 Summary ......................................................... 145

7 Future Work and Conclusions ................................ 147
  7.1 Future Work .................................................. 147
    7.1.1 DPC Based IR-UWB Receiver Architectures .... 148
    7.1.2 DPC Based IR-UWB RAKE Receiver Architecture .. 149
  7.2 Conclusions ................................................ 150

Bibliography ...................................................... 152
List of Tables

4.1 Impulses generated by the single-polarity DWG prototype ........ 90
4.2 Performance summary of the single-polarity DWG prototype ........ 93
4.3 Comparison of the single-polarity DWG prototype with other reported work .......................................................... 93
4.4 Impulses generated by the dual-polarity DWG prototype ........ 99
4.5 Performance summary of the DWG based IR-UWB transmitter ... 106
4.6 Performance comparison with other reported high-speed DACs .... 106
List of Figures

1.1 Channel capacity vs. bandwidth for additive white Gaussian noise channels. .............................................. 3
1.2 Data rate vs. bandwidth in today’s wireless communications. ........ 3
1.3 $f_T$ and $f_{max}$ trends of CMOS, SiGe BiCMOS and III-V semiconductors. 5
1.4 Design tradeoffs in digital and analog/RF integrated circuits. ....... 6
1.5 Supply voltage and threshold voltage scaling trends in CMOS tech-
nologies. .......................................................... 7
1.6 Frequency band allocation for UWB systems. ................. 8
1.7 FCC power emission mask for UWB systems. .................. 9
1.8 Modulation schemes for IR-UWB communications. .......... 10
1.9 Multi-band OFDM UWB. ..................................... 11
1.10 Pulse filtering circuits in a laser system. ...................... 12
1.11 ACSL system for pulse filtering in laser system. ............ 12

2.1 A common-source amplifier. .................................. 18
2.2 A shunt-peaked amplifier. ...................................... 18
2.3 A series-peaked amplifier. ...................................... 19
2.4 A shunt-series amplifier. ....................................... 20
2.5 Two differential pairs as the $f_T$ doubler. .................... 21
2.6 A capacitively degenerated differential pair. .................. 22
2.7 A cherry-hopper amplifier. .................................... 23
2.8 A balanced amplifier using 90-degree hybrid couplers. ....... 24
2.9 Single-stage amplifier (a) First-order load (b) General passive impedance load. ................................. 25
2.10 A distributed amplifier. ................................................. 27
2.11 A generic distributed architecture. ................................. 28
2.12 Distributed circuits expand the design space by introducing circuit complexity as a parameter. ......................... 28

3.1 A conventional constant-k DA (bias not shown). ................. 32
3.2 The proposed DA with non-uniform filtering (bias not shown). ... 33
3.3 Model of a generic DA with non-uniform filtering structures, showing the \( i \)-th tap. For simplicity, gate and drain lines are assumed to be identical. ........................................ 33
3.4 Comparison of DAs with different filtering functions (simulated): (a) magnitude response (b) phase response. ................. 34
3.5 Normalized design parameters for both filtering structures implemented as LC artificial transmission lines. ......................... 36
3.6 Circuit schematic of the prototype DAs. ............................. 37
3.7 Chip micrographs of the prototype DAs. ............................. 38
3.8 Measured performance of the prototype Butterworth DA: (a) power gain; (b) phase response; (c) input return loss; (d) output return loss. 39
3.9 Measured performance of the prototype Chebyshev DA: (a) power gain; (b) phase response; (c) input return loss; (d) output return loss. ... 40
3.10 Input IP3 and 1dB compression point of the prototype DAs. ....... 41
3.11 An FIR transversal filter. ................................................. 43
3.12 A distributed transversal filter. ........................................ 43
3.13 (a) LC line ladder structure; (b) generic ladder structure. ....... 46
3.14 Ladder structure for the drain line. ................................. 46
3.15 Circuit schematics. (a) 5-tap DTF ; (b) gain cell. .................. 51
3.16 Simulated waveforms. (a) square pulse; (b) Gaussian pulses. .... 53
3.17 Chip micrograph of the 5-tap prototype DTF. ...................... 54
3.18 Frequency response of each tap in the prototype DTF. .......... 55
3.19 Pulse response of each tap in the prototype DTF. .......... 55
3.20 Gain control linearity of each tap in the prototype DTF. ...... 55
3.21 Measured waveforms synthesized using the prototype DTF. (a) square pulse; (b) Gaussian pulses. ......................... 56
3.22 A DTF with the new gain cell design including both digital controls and analog tuning. ................................. 59
3.23 (a) Binary-weighted gain cell, each digital bit controls a number of identical unit cells. (b) Each unit cell is implemented as a current-steered quasi-differential amplifier with tail current tuning. 61
3.24 Chip micrograph of the prototype DTF with binary-weighted gain cells. 62
3.25 Measured frequency responses of each tap. .................. 63
3.26 Measured frequency responses of tap1 with digital control. .... 64
3.27 Impulse response of each tap in the prototype DTF. The interstage delay is 48.6 ps, 49.9 ps, 51.5 ps, 50.5 ps. .................. 65
3.28 Tuning of each tap in the prototype DTF: (a) Pulse amplitude; (b) Correlation factor. ................................. 65
3.29 Generated UWB waveforms and spectra using the prototype DTF. 66
3.30 The delay-bandwidth tradeoff in DTF ......................... 67

4.1 UWB spectrum: (a) UWB band allocation with other existing wireless networks including WiMax; (b) UWB emission mask of different regions. 71
4.2 Current IR-UWB pulse generation approaches: (a) up-conversion; (b) passive filters; (c) high-speed DAC. Both generated waveforms and pulse spectra are shown in each approach. Note that in the DAC approach, the spectrum in discrete time domain is periodic over the sampling frequency $f_s$. ....................... 74
4.3 UWB pulse characteristics. .................................. 76
4.4 Distributed waveform generator architecture. ................. 78
4.5 Different sampling schemes to generate UWB pulse: (a) Nyquist sampling; (b) peak sampling; (c) spectra of the sampled signal using these two sampling schemes. ................ 80
4.6 Similar to (a) a generic transversal filter, a DWG can be considered
(b) a transversal filter with the signal source embedded. ............... 81
4.7 IR-UWB pulses and spectra generated using FIR filter (a) $\tau=130$ ps
and $N=20$; (b) $\tau=80$ ps and $N=10$. ................................. 82
4.8 (a) OOK and (b) PPM modulations are performed on the trigger signal
in DWG. ................................................................. 84
4.9 Overall schematic of the single-polarity DWG prototype. ........... 86
4.10 Schematic of the single-polarity DWG prototype: (a) active delay line;
(b) impulse generator; (c) switched current source. ............. 87
4.11 Chip micrograph of the prototype single-polarity DWG. The mean-
dered output transmission line is connected between two RF pads.
The pads at the lower-half chip are for tuning controls and dc bias. 88
4.12 Pulses generated by each tap. ........................................... 89
4.13 (a) Pulse width tuning (showing only tap1); (b) Delay tuning (showing
only tap1 and tap2). .................................................. 90
4.14 (a) Pulse amplitude tuning and (b) corresponding pulse shape change. 90
4.15 Example waveforms synthesized using the prototype DWG........ 92
4.16 Output waveform of the prototype DWG driven by PRBS data. ... 92
4.17 Proposed IR-UWB transmitter. ....................................... 94
4.18 Overall schematic of the dula-polarity DWG based IR-UWB transmitter 95
4.19 Schematic of the dual-polarity DWG based IR-UWB transmitter: (a)
impulse generator; (b) dual-polarity switched current source; (c) pulse
position modulator. ................................................................. 96
4.20 Chip micrograph of the prototype IR-UWB transmitter. .......... 97
4.21 Impulses generated by all DWG taps in the prototype transmitter,
showing only the negative pulses. ........................................... 98
4.22 (a) impulse width tuning and (b) tuning tap delay, showing only im-
pulses from tap1 and tap2. ........................................ 99
4.23 Some measured UWB waveforms and their spectra from the dual-
polarity DWG based transmitter. ..................................... 101
4.24 OOK modulation using 32 Mbps PRBS data. ....................... 102
4.25 Measured output waveforms at 2.5 GHz, 1.5 GHz and 500 MHz pulse rate. .................................................. 103
4.26 Tunable Δ-PPM from 200 ps to 400 ps. ................................. 104
4.27 Measured PPM output waveforms modulated at 40 MHz, driven at 200 MHz. .................................................. 105
4.28 Overall schematic of the 64-tap DWG. ................................. 107
4.29 Schematic of the prototype DWG: (a) DAC assisted pulse generator;
(b) pulse generator array; (c) new current-steering pulse generator. 108
4.30 Chip micrograph of the 64-tap DWG. ................................. 109
4.31 Pulses generated by each tap in 64-tap DWG prototype. ............ 110
4.32 Rise time of all 64 taps. .................................................. 110
4.33 Using Tap1 as example (a) Pulse amplitude tuning and (b) correspond-
ing pulse shape change. .................................................. 111
4.34 Jitter performance of some taps. ....................................... 112
4.35 Some example waveforms generated using the DWG prototype. (a)
using tap1,2,3; (b) using tap1to tap10. .................................... 113
4.36 Proposed IR-UWB transmitter with M-ary pulse shape modulation. 114
4.37 Schematic of the DWG based IR-UWB transmitter with binary pulse
shape modulation. ...................................................... 115
4.38 (a) Schematic of the DAC-assisted pulse generator; (b) dual-polarity
switched current source. ................................................ 116
4.39 Chip micrograph of the prototype IR-UWB transmitter with pulse
shape modulation. ...................................................... 117
4.40 Pulses generated by each tap in one 20-tap DWG. ..................... 117
4.41 (a) Generated pulses with BPSK modulation; (b) Generated pulses
with PSM. .................................................................. 118
4.42 (a) Generated orthogonal pulses for PSM; (b) (c) Measured spectra of
the two orthogonal pulses. .......................................... 119
5.1 IR-UWB receiver architecture based on conventional analog correla-
tion. ................................................................. 123
<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.2</td>
<td>IR-UWB transceiver architecture based on DWG and DPC.</td>
<td>124</td>
</tr>
<tr>
<td>5.3</td>
<td>A distributed pulsed correlator (DPC).</td>
<td>125</td>
</tr>
<tr>
<td>5.4</td>
<td>Overall schematic of the differential DPC prototype.</td>
<td>126</td>
</tr>
<tr>
<td>5.5</td>
<td>Schematic of the pulsed multiplier with built-in impulse generator.</td>
<td>127</td>
</tr>
<tr>
<td>5.6</td>
<td>Simulation results of the DPC prototype.</td>
<td>127</td>
</tr>
<tr>
<td>5.7</td>
<td>Chip micrograph of the DPC prototype.</td>
<td>128</td>
</tr>
<tr>
<td>5.8</td>
<td>Setup of the DPC test.</td>
<td>130</td>
</tr>
<tr>
<td>5.9</td>
<td>Measured differential input waveforms to the DPC prototype, generated by the LNA from a single-ended Gaussian-shape pulse.</td>
<td>130</td>
</tr>
<tr>
<td>5.10</td>
<td>Measured correlator outputs from the DPC prototype.</td>
<td>131</td>
</tr>
<tr>
<td>5.11</td>
<td>Measured DPC outputs with 200ps timing offset.</td>
<td>132</td>
</tr>
<tr>
<td>5.12</td>
<td>Measured DPC outputs with different templates.</td>
<td>132</td>
</tr>
<tr>
<td>5.13</td>
<td>Measured DPC outputs using same amplitude templates with opposite polarity.</td>
<td>133</td>
</tr>
<tr>
<td>6.1</td>
<td>CPW directional couplers (not to scale). (a) edge-coupled; (b) broadside-coupled.</td>
<td>137</td>
</tr>
<tr>
<td>6.2</td>
<td>Broadside-coupled CPW directional coupler in a digital CMOS process.</td>
<td>139</td>
</tr>
<tr>
<td></td>
<td>(a) Cross section; (b) top view.</td>
<td></td>
</tr>
<tr>
<td>6.3</td>
<td>Electric fields of possibly excited modes: (a) dominant quasi-TEM mode; (b) coupled slot-line mode; (c) parasitic substrate mode; (d) parasitic waveguide mode.</td>
<td>140</td>
</tr>
<tr>
<td>6.4</td>
<td>Phase factors of possibly excited modes.</td>
<td>141</td>
</tr>
<tr>
<td>6.5</td>
<td>Die micrograph of the directional coupler.</td>
<td>142</td>
</tr>
<tr>
<td>6.6</td>
<td>Measured impedance levels of two feed lines.</td>
<td>142</td>
</tr>
<tr>
<td>6.7</td>
<td>Measured and simulated s-parameters of the coupler: (a) Through (S21) and Coupling (S31); (b) Matching (S11) and Isolation (S41).</td>
<td>143</td>
</tr>
<tr>
<td>6.8</td>
<td>Measured phase response of the coupler.</td>
<td>144</td>
</tr>
<tr>
<td>6.9</td>
<td>Measured directivity of the coupler.</td>
<td>144</td>
</tr>
<tr>
<td>7.1</td>
<td>DPC based IR-UWB receiver architecture for PPM.</td>
<td>147</td>
</tr>
<tr>
<td>7.2</td>
<td>DPC based IR-UWB receiver architecture for PSM.</td>
<td>148</td>
</tr>
</tbody>
</table>
7.3 DPC based IR-UWB RAKE receiver architecture. 149
Chapter 1

Introduction

In the past a few years, personal mobile networks and wireless broadband internet access, has led a new ubiquitous time of wireless communications [1]. Achieving the highest performance of wireless systems, such as speed, power and functionality, is the primary focus of today’s radio engineers. With such promising prospects, wideband/high-speed integrated circuits have become one of the most active research areas with strong industry demands and fast technological progresses [2].

1.1 Performance Issues in Wireless Communications

Following the history of communications, higher data rate is always the main target to pursue in wireless communication system design. Besides of high data rate, low power consumption, or in other words, high power efficiency becomes increasingly critical in wireless communications because of the popularity of battery-powered wireless devices [3]. This section will briefly discuss some performance issues in wireless communication systems, including bandwidth, data rate, power efficiency and system reconfigurability.
1.1.1 Bandwidth and Data Rate

Operation frequency is one of the most important properties of communication integrated circuits since a higher operation frequency is an evident method of achieving larger bandwidth and higher data rate in many communication systems. In communication systems, data rate usually refers to the information transmission at the baseband in unit of bit per second while the bandwidth refers to the radio frequency (RF) front-end circuits in unit of Hz. These two terms are theoretically related. RF bandwidth is from half of the data rate to zero frequency according to the Nyquist Sampling Theorem and has some overhead in practice.

One performance measure of a radio in applications such as communications, tracking and locating, is the channel capacity for a given bandwidth and signal-to-noise ratio (SNR). Channel capacity is the theoretical maximum limiting number of bits per second information that can be transmitted through a given channel with arbitrarily low error probability.

For an additive white Gaussian noise channel, Shannon-Hartley Theorem expresses the channel capacity \( C \) as \[ 4 \]

\[
C = B \log(1 + SNR)
\] (1.1)

where \( C \) is the channel capacity of point-to-point communications, \( B \) is the bandwidth and \( SNR \) is the signal-to-noise ratio. \( SNR \) can be further related to the bandwidth as

\[
SNR = \frac{P_{sig}}{N \cdot B}
\] (1.2)

where \( P_{sig} \) is the signal power and \( N \) is the noise power spectrum density. In most wireless communication channels, \( N \) is the thermal noise floor, which is \(-174dBm/Hz\).

The Shannon theorem actually implies several ways to achieve high data rate which is fundamentally limited by the channel capacity. One way is to increase the SNR by transmitting larger signal power. But this usually consumes more power and may cause interference problems with other wireless network. Another way is to use advanced modulation, coding and multiple access techniques. This would basically
Figure 1.1: Channel capacity vs. bandwidth for additive white Gaussian noise channels.

Figure 1.2: Data rate vs. bandwidth in today’s wireless communications.

push the data rate closer to the channel capacity limit. Recently, multiple-input and multiple-output (MIMO) technique has been proposed to increase the data rate and link range without additional bandwidth or transmit power by using multiple antennas at both the transmitter and receiver. However, these techniques improve communication performance at the cost of system complexity and power consumption.

Another simple way to increase the data rate is to use larger bandwidth. The relation between channel capacity and bandwidth can be visualized in Fig.1.1. Even though the channel capacity will be eventually saturated due to the noise limit, bandwidth is still an effective way to improve data rate considering the thermal noise power is not large enough for the normal radio frequency range. To the first order, the data
rate is proportional to the signal bandwidth when the noise power is small. Increasing bandwidth for higher data rate is also a popular solution for today’s most wireless communication systems, as shown in Fig. 1.2

1.1.2 Power Efficiency

As the data rate and communication system complexity increase, the power consumption becomes more critical, which is especially true for wireless communications. Most wireless devices are battery-powered due to the mobility requirement. Thus, power optimization for high efficiency is another major concern of designing wireless communication circuits [5]. Power efficiency is a better description for the performance than simply low power, because higher power efficiency means the same amount of power can be used to implement more functions, which are also desired for modern mobile devices, such as cell phones. Novel designs from different levels (architecture, circuit, device, etc.) in a system are needed to achieve this goal. While the process technologies set a fundamental limit on the power consumption, architecture and circuit innovations can enable the use of low-cost technologies to achieve power consumption comparable to those achieved using advanced technologies.

1.1.3 System Reconfigurability

System Reconfigurability is another attractive characteristic for communication systems [6]. After fabrication and integration, it is desired that the system can be reconfigured to adaptively satisfy different communication standards. For example, the same cell phone can support multiple cellular standards (GSM, CDMA), wireless internet (WiFi, WiMax), Bluetooth for the headset and GPS for localization. Communication systems also need to work at different modes for different tasks, so that usage of communication resources can be adaptively optimized. In order to accommodate process variations, regulatory difference, changes in channel and antenna characteristics, systems also need to be reconfigurable for different communication environments [7].
Figure 1.3: $f_T$ and $f_{\text{max}}$ trends of CMOS, SiGe BiCMOS and III-V semiconductors.

1.2 Challenges in CMOS RF Integrated Circuits

Silicon-based integrated circuits (ICs) play a central role in the evolution of the wideband/high-speed radio frequency (RF) circuits and systems. The major advantage of silicon technologies, especially CMOS, is the extremely large integration capability that enables the implementation of system-on-chip (SOC) at very low cost. For example, in today’s CMOS technologies, more than 10,000 transistors can be integrated on one chip, and this number doubles every 18 months, while dropping the price of each transistor by a factor of 100 over 15 years.

Besides cost issue, large scale integration has two other advantages. First, since different function blocks are now built on the same chip, the parasitic effects of packages and printed circuit boards (PCBs) on the interface between them are removed. Therefore, the operation speed can be significantly higher as the speed is only limited by the on-chip devices and interconnects. Second, the power consumption associated with input/output drivers which are required at the interface between chips in a multi-chip environment, will be eliminated.

The scaling trend of silicon technologies enables the implementation of microwave/
millimeter-wave integrated circuits (MMICs) in silicon. Fig. 1.3 shows the projections of International Technology Roadmap for Semiconductors on CMOS, SiGe technologies [8], in terms of maximum unity current gain frequency $f_T$ and maximum unity power gain frequency $f_{max}$. For comparison, the performance of III-V compound semiconductors is also shown in the figure. As can be seen, the silicon technologies has pushed the cut-off frequency ($f_T$) of NMOS transistors to over 150 GHz at 90 nm technology node and beyond 200GHz at 65 nm [9]. These technology progresses make silicon capable of delivering more functionality at a lower price, and also become a preferable candidate for low-cost wideband/high-speed integrated circuits.

There are many challenges in high-speed integrated circuit design for applications like those in the previous section because of the fundamental physical limitations. First, the cutting-edge specifications required by advanced communication systems still exceed the capabilities of current CMOS technologies using conventional wideband circuit design techniques [10]. The development of current CMOS technologies are mainly driven by the very-large-scale integrated (VLSI) systems such as microprocessors. The optimization of most CMOS technologies only involves one design tradeoff between speed and power, while for analog/RF design more design tradeoffs are included. As shown in Fig. 1.4, almost every two design parameters can be traded with each other.

Technology scaling also presents challenges for high-speed analog/RF design. As shown in Fig. 1.5, as CMOS technologies scale down to smaller feature size, the voltage headroom between supply voltage and threshold voltage is becoming smaller. The
low supply voltage in the deep-submicron process (1.5V or lower) and relatively high threshold voltage (0.5V or higher) severely limit the signal-to-noise ratio and dynamic range of RF circuits [11]. Therefore, it is desired to develop new architecture and circuit techniques that can achieve wideband/high-speed operations with low power consumption and wide dynamic range using low cost CMOS technologies.

Another challenge is the quality of on-chip passive components, such as inductors, capacitors and transmission lines. In CMOS technologies, the low-resistivity substrate (~10 mΩ·cm) is usually adopted with a thin epitaxial layer. This low-resistivity substrate increases the electromagnetic coupling between the devices and silicon substrate. This can significantly degrade the performance of on-chip passive components due to the capacitive coupling and dielectric loss. For example, widely-used spiral inductors can suffer from low self-resonance frequency, low Q-factor, and another issue more problematic in wideband circuit design which is that the inductance value can not maintain constant with larger bandwidth [12].

Accurate models of transistors and passive components in microwave/millimeter-wave frequency range are still lacking [13]. Compared to the fast progress of CMOS technologies, theoretical understanding of device physics and computer-aided design (CAD) modeling for these deep submicron transistors are still under development. At high frequency, distributed effect of on-chip passive components becomes evident and
Figure 1.6: Frequency band allocation for UWB systems.

requires accurate electromagnetic simulations for modeling. Therefore, new circuit
design techniques have to take these constraints into account.

1.3 Applications of Ultra-Wideband Pulse Processing

The generation, detection and filtering of ultra-wideband pulses have become increasingly important in wireless communications, fiber-optical communications [14]
[15], high-speed instrumentation and pulse radar systems [16]. This section will
present two example applications: impulse radio ultra-wideband communications and
pulse filtering in laser systems.

1.3.1 Impulse Radio UWB Communications

Ultra-Wideband (UWB) may be used to refer to any radio technology having
bandwidth exceeding lesser of 500MHz or 20% of the arithmetic center frequency, ac-
cording to Federal Communications Commission (FCC) [17]. The world of UWB has
attracted dramatic attention in recent years. In the past 20 years, UWB was used for
radar, sensing, military communications [18]. A substantial change occurred in Febru-
ary 2002, when the FCC issued that UWB could be used for data communications
as well as for imaging and location applications.
Figure 1.7: FCC power emission mask for UWB systems.

The band allocated to communications is from 3.1 GHz to 10.6 GHz, a staggering 7.5 GHz, by far the largest allocation of bandwidth to any commercial terrestrial system (Fig. 1.6). This enormous bandwidth means that UWB could potentially offer data rates on the order of Gbps. But because many other frequency bands of existing wireless systems are also allocated within this 7.5 GHz band, these yield the concern on interference problems between UWB and other wireless systems. The concession from UWB communications was that available power levels would be very low (Fig. 1.7). The power spectrum density is $-41.3\, dBm/MHz$, which implies that if the entire 7.5 GHz band is fully utilized the maximum power available to a transmitter is approximately 0.5mW. This is a very small fraction of what is available to users of the 2.45 GHz ISM bands such as the IEEE 802.11 a/b/g standards. This emission power limit effectively regulates UWB to short-range, high data rate communications or low data rate for longer link distances[19]. One of the potentials of UWB is the capability of transition between the high data rate, short link distance and the very low data rate, longer link distance applications [20], which implies that the variable data rate transceiver is needed to support this transition capability physically.

For UWB communications, there are two technologies used for system implementation, impulse radio and multiband [21] [22]. The impulse radio UWB (IR-UWB)
is the original approach to UWB by using narrow pulses that occupy a large portion of the spectrum. The work about UWB communication circuits and systems in this dissertation falls into the scope of IR-UWB. IEEE 802.15.4a standardization committee has recently been formed to propose an IR-UWB based physical layer to enable data communications and high precision ranging/location capability (1 meter accuracy and better), high aggregate throughput and ultra low power; as well as adding scalability to data rates, longer range, and low power consumption and cost [23]. Because of the usage of very short pulses for data transmission, the IR-UWB transceiver circuits are essentially used to implement functions such as generation, modulation, filtering and detection of UWB pulses. Several modulation schemes are shown in Fig. 1.8, including on-off keying (OOK), binary phase shift keying (BPSK), pulse position modulation (PPM) and pulse shape modulation (PSM). OOK and BPSK are widely adopted modulation schemes for digital modulation. PPM is a special modulation scheme proposed for IR-UWB. Because very short pulses (1-2ns) are used to transmit data, the information can be carried on the position where the UWB pulse is located. PSM employs a set of orthogonal pulse shapes for data transmission which can potentially achieve higher data rate in a multipath channel compared to other modulation schemes.

The multiband approach divides the available UWB spectrum into totally 14
smaller and nonoverlapping bands and use orthogonal frequency division multiplexing (OFDM) [24]. The band division and band selection of different regions are shown in Fig. 1.9. Each band has a bandwidth of 528 MHz to obey the FCC’s definition of UWB signals. Information is transmitted via 128 subcarriers in each band using quadrature phase-shift keying (QPSK) modulation. This approach takes advantage of frequency diversity while delivering necessary robustness against interference and multipath, even in the most challenging channel environments. Dividing the UWB spectrum into multiple frequency bands offers the advantage of avoiding transmission over certain bands, such as 802.11a at 5 GHz, to prevent potential interference. This offers better coexistence with other radio services. Such a multiband OFDM system has a similar architecture as the conventional RF system. This is an advantage because OFDM has been widely adopted by other standards organizations, including ADSL, 802.11a/g, 802.16a, digital audio broadcast, and digital terrestrial television broadcast.

IR-UWB has a number of advantages that make it attractive for communication applications. In particular, IR-UWB systems have potentially low complexity and low cost, which arises from the essentially baseband nature of the signal transmission. Since IR-UWB signal spans frequencies commonly used as carrier frequencies, the signal will propagate well without additional up-conversion and amplification. The reverse process of down-conversion is also not required in the IR-UWB receiver. This means the local oscillator, mixer and associated complex delay and phase locked loops
might be removed from the receiver.

Due to the low emission power density and the pseudo-random characteristics of the transmitted signal, the UWB signal is noise like, so the unintended detection is quite difficult. The wide bandwidth and noise like signals are resistant to severe multipath and jamming effects. UWB systems also have very good time domain resolution allowing for location and tracking applications.
1.3.2 Pulse Filtering in Laser Systems

The other motivation of UWB pulse generation and filtering is from the pulse shaping application in laser systems. Due to the ultra-fast nature of laser system, pulse shaping circuits need to provide pulses with multi-GHz bandwidth and very fast rise/fall time, even though the power consumption is not the major concern in this case.

OMEGA laser system at LLE is one of the most powerful and highest energy lasers in the world. It is a 60-beam pulsed ultraviolet (UV) neodymium glass laser. Its 60 laser beams focus up to 40 kilojoules of optical energy onto a target that measures less than 1 millimeter in diameter in approximately 1 nanosecond, which corresponds to about 40 terawatts in terms of power. OMEGA provides a unique capability to conduct inertial-confinement, direct-drive, laser-induced fusion experiments and other basic physics experiments in support of the National Inertial Confinement Fusion (ICF) program. The ultimate goal of LLE experimental program on OMEGA is to achieve controlled nuclear fusion, which will provide a safe, clean, and virtually unlimited source of energy. OMEGA is also used to develop new materials and laser technologies, and other advanced technologies related to high-energy-density phenomena.

Based on fusion experiment requirements, OMEGA needs to generate optical pulses with various temporal pulse shapes. This is done by inserting an electric-optical modulator in the laser system, and applying a shaped electrical pulse to modulate the optical pulse, as shown in Fig. 1.10. The shaped electrical pulse is generated by a pulse generator with a fixed pulse shape output, and then changed to the target pulse shape by a pulse filtering circuit. The difficulty of such a pulse shaping circuit lies in the stringent requirement on its output waveform, including fast rise/fall time, accurate time/amplitude resolution, and relatively long pulse width. The shaped electrical pulse needs 100 ps time resolution, 20 dB dynamic range and more than 1 ns pulse duration. The pulse shape is usually different from shot to shot, and hence it is highly desirable that the pulse filtering circuit can be reconfigured adaptively.

Currently, pulse filtering in OMEGA is implemented as an aperture-coupled stripline
(ACSL) module [25], shown in Fig. 1.11. There are two transmission lines (specifically, striplines) in this module, one for the input pulse, and the other for the output. Both are terminated at one end. There is an opening (aperture) at the middle ground layer. When the input pulse propagates along the input line, it is coupled to the output line through the aperture. The aperture width determines the coupling strength, and its length corresponds to the output pulse duration. By designing the geometry of the coupling aperture, a specific electrical pulse shape can be generated. The main advantage of this approach is its simplicity. It is a passive microwave device with well-understood characteristics. And it can achieve the function reasonably well – as long as the other parts of the system have a stable, known impulse response. The disadvantages are: 1) since it is a passive circuit, it introduces loss and thus reduces the pulse amplitude and lower its SNR; 2) it is difficult to construct and tune since any change could possibly mean another PCB; 3) it lacks adaptability, and hence cannot follow any change in the required pulse shape or variations in the system; 4) it can be costly in the long run because of 2) and 3).

Therefore, it is highly desirable for the pulse filtering circuit to be reconfigurable so that we can (adaptively) change the spectrum/waveform according to varied target pulses like in the OMEGA system. Ideally, we want to implement such a pulse filtering circuit using standard CMOS technologies, because of their potential for integration with digital signal processing (DSP) circuitry and low cost.

1.4 Contributions of This Dissertation

To overcome these challenges, this dissertation proposes an idea to trade circuit complexity for speed, power and dynamic range by utilizing the large scale integration capabilities in CMOS. We developed several new architectures and circuit techniques along with design methodologies, namely, distributed waveform generators (DWG) and distributed pulsed correlators (DPC), for ultra-wideband pulse generation and detection. New design concepts were also introduced into the distributed amplifier (DA) and distributed transversal filter (DTF) design for ultra-wideband pulse filtering. Digitally-assisted circuit technique was also applied into the DWG and DTF
design to improve the dynamic range. Wideband directional coupler in CMOS environ-
ment was implemented based on innovative electromagnetic design techniques.

Two DA prototypes with Butterworth and Chebyshev filtering were implemented
using the concept of network synthesis method. A 5-tap DTF prototype with 50ps
time resolution was implemented for sub-nanosecond pulse synthesis with 80ps rise
time. The trading of circuit complexity for high-speed and low power consumption
has been experimentally demonstrated using a 10-tap, 10GS/s single-polarity DWG
prototype with digital pulse generators. For low-power IR-UWB applications, a 10-
tap, 10GS/s, dual-polarity DWG with pulse position modulator was implemented
as the transmitter with 3-9GHz bandwidth and 45pJ/pulse power efficiency. A 8-
tap, 10GS/s differential DPC prototype has been implemented as the RF front-end
circuit of a IR-UWB receiver, which achieves 40pJ/b with 250Mbps data rate in the
measurement. To trade circuit complexity for accuracy, digital-to-analog converters
(DAC) assisted pulse generators were incorporated into a 10.9GS/s DWG prototype to
achieve more than 20dB dynamic range of pulse generation. Binary-weighted gain cell
design was adopted in a DTF prototype for enhancing the dynamic range of wideband
filtering. Measurement results successfully demonstrate the new architecture and
circuit techniques.

1.5 Dissertation Organization

This dissertation begins with the background knowledge in Chapter 2 about con-
ventional wideband circuit design techniques and basic distributed amplifiers and
architectures. Chapter 3 will present the distributed pulse filtering circuits, includ-
ing the DAs with Butterworth/Chebyshev filtering functions and the DTF with two
prototypes for pulse filtering in laser systems and IR-UWB communication systems,
respectively. Chapter 4 will present the DWG architecture and circuit techniques as
a new approach for ultra-wideband pulse generation with built-in filtering functions
and modulation capabilities. The detailed design of three circuit prototypes will be
discussed, including a 10-tap, 10GS/s single-polarity DWG, a 10.9GS/s DWG pro-
totype with DAC-assisted current-steering pulse generators and a 10-tap, 10GS/s,
dual-polarity DWG with pulse position modulator. Chapter 5 will discuss the DPC architecture and a differential DPC prototype for ultra-wideband pulse detection in IR-UWB receivers. Chapter 6 will present the 10-40GHz wideband directional coupler as the initial investigation into implementing millimeter-wave integrated circuits in standard digital CMOS technologies. Chapter 7 will conclude this dissertation with some words about future work.
Chapter 2

Conventional Wideband Circuit Techniques

The design of circuits with large bandwidth needs more detailed considerations than narrow-band circuits [26][27]. Limitations may come inherently from active devices themselves. The speed of a transistor in a given technology is usually characterized by its unity-gain frequency shown as \( f_T \). This is the frequency at which the current gain of a transistor drops to unity. Usually analog circuits operate at frequencies 3-100 times smaller because they rely on closed loop operation based on negative feedback and have to operate at a frequency lower than the \( f_T \) to provide enough gain [28] [29]. Additionally, parasitic capacitances and inductances can impose serious constraints on achievable bandwidth. The combination of these two effects significantly reduces the maximum operation frequency in most conventional circuits, and provides a motivation to pursue circuit design techniques to alleviate the bandwidth limitations.

In this chapter, several conventional bandwidth enhancement techniques will be discussed firstly [30]. Then gain-bandwidth product (GBW) will be introduced to derive the theoretical limit and design trade-offs for wideband amplifier design. After that, the basic principle of distributed amplifiers will be explained.
2.1 Wideband Amplifier Design

2.1.1 Shunt-Peaked Amplifiers

As shown in Fig 2.1, in a common-source amplifier, the bandwidth is determined by the RC time constant associated with $R$ and $C$ which represents all the loading resistance and capacitance on the output node. Because a capacitive load is added, the gain eventually falls off as frequency increases because the capacitor’s impedance diminishes.

One approach to compensate the capacitive load, known as shunt peaking, is to add an inductance in series with the load resistor, as in Fig. 2.2. This can provide an
impedance component that increases with frequency which helps pull up the decreasing impedance of the capacitive load, yielding a net impedance then remains roughly constant over a wider frequency range than that of the original RC load.

The gain of the shunt-peaked amplifier is the product of $g_m$ and the magnitude of the RLC network impedance, which is

$$|Z(j\omega)| = R \sqrt{\frac{(\omega L/R)^2 + 1}{(1 - \omega^2 L C)^2 + (\omega R C)^2}} \quad (2.1)$$

In contrast with the simple RC case, there is a term in the numerator (forms the zero) that increases with increasing frequency. Furthermore, the $1 - \omega^2 L C$ term in the denominator contributes to an increase in $|Z|$ for frequencies below the LC resonance as well. Both of these terms extend bandwidth.

### 2.1.2 Series-Peaked Amplifiers

In the shunt-peaked amplifier, the output capacitance actually includes two parts: the load capacitance and the drain capacitance of the transistor. In designs where the drain capacitance is significant, better bandwidth extension can be achieved by inserting an inductor between the drain capacitance and the load capacitance to split them. To understand this capacitive splitting effect, consider the series-peaked
amplifier shown in Fig. 2.3. The voltage transfer function of this amplifier is

\[ H(j\omega) = g_m \cdot \frac{j\omega RC_1}{R + j\omega C_1 - \omega^2 R L C_2 - \omega^2 R C_1 C_2 - j\omega^3 C_1 L C_2} \]  \hspace{1cm} (2.2)

As expected, the separation of \( C_1 \) and \( C_2 \) creates another pole which affects the bandwidth. Additional insight into the capacitive splitting can be gained by considering the unit step response of the amplifier. Instead of charging \( C_1 + C_2 \) without \( L \), the transistor charges \( C_1 \) only initially with \( L \) because \( L \) delays current flow to the rest of the network. This reduces the rise time at the drain, thus increases the bandwidth.

### 2.1.3 Shunt-Series Amplifiers

Another approach to the design of wideband amplifiers is to use negative feedback, particularly shunt-series amplifier. The shunt-series amplifier is depicted in Fig. 2.4. Assuming that \( R_1 \) is large enough relative to the reciprocal of the transistor's \( g_m \), and \( R_F \) is large enough that its loading on the output node may be neglected, the voltage gain of the amplifier from the gate to the drain is approximately \(-\frac{R_L}{R_1}\).

Although \( R_F \) is assumed to have little effect on gain, it can reduce both input and output resistances through the shunt feedback it provides. The reduction of input and output resistances helps to increase the bandwidth further by reducing the
open-circuit time-constant. Formally, $R_{in}$ is given by

$$R_{in} = \frac{R_F}{1 - A_V} \approx \frac{R_F}{1 + R_F/R_1} \tag{2.3}$$

And $R_{out}$ is given by

$$R_{out} = \frac{R_F + R_S}{1 + R_S/R_1} \approx \frac{R_F}{1 + R_S/R_1} \tag{2.4}$$

The ease of providing a simultaneous impedance match at both input and output ports is a desired property for wideband amplifier, especially at RF and microwave frequencies.

### 2.1.4 $f_T$ Doubler

Considering the equation for $f_T$, which is

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{2.5}$$

To increase $f_T$, we can either increase transconductance $g_m$ or reduce the gate-source capacitance $C_{gs}$. For the same bias current, we can reduce the transistor width and increase the overdrive voltage to achieve higher $f_T$. 
Another bandwidth enhancement technique is the $f_T$ doubler as shown in Fig. 2.5. In this case, the overall voltage gain of two differential pairs is the same as the gain in a single differential pair. However, the input capacitance is reduced by half because two gate-source capacitances are connected in series, which essentially double the $f_T$. The disadvantages of such a topology include the doubled total power consumption and larger voltage drop on the load resistors.

### 2.1.5 Capacitive Degeneration

In order to extend the bandwidth, it is possible to degenerate the transistor to have increased equivalent transconductance as the operation frequency increases. Therefore, it can compensate the high frequency roll-off and result in bandwidth enhancement. The schematic of a capacitive degenerated differential pair is shown in Fig. 2.6. Based on the half-circuit concept, the voltage gain is expressed as

$$A_v = \frac{g_m R (s C_d R_d + 1)}{(1 + s R C) (g_m R_d / 2 + 1 + s C_d R_d)}$$  \hspace{1cm} (2.6)
The voltage gain has a zero at $1/(R_dC_d)$, and two poles at $1/(RC)$, $(g_mR_d/2 + 1)/(R_dC_d)$. By proper selection of the degeneration capacitance $C_d$, the frequency peaking can be located at the target frequency band. The zero can be used to cancel the dominant pole, resulting in bandwidth extension. For on-chip implementations, the accuracy of capacitors usually suffers from the process variations. Large chip area of capacitors also limits the application of this technique.

### 2.1.6 Cherry-Hopper Amplifiers

The cherry-hopper amplifier has been used as a bandwidth enhancement circuit topology based on local shunt-shunt feedback. Fig. 2.7 shows a Cherry-Hopper amplifier with ideal current source load. The voltage gain of this Cherry-Hopper amplifier can be calculated to be

$$A_v = g_{m1}(R_F - \frac{1}{g_{m3}})$$  \hspace{1cm} (2.7)

As far as $R_F$ is much larger than $1/g_{m3}$, the gain is the same as a differential pair with load $R_F$. At the same time, the output impedance of the Cherry-Hopper amplifier is approximately $1/g_{m3}$, which is usually much smaller than the MOS transistor drain resistance, yielding the output pole located at much further away from the origin.
Figure 2.8: A balanced amplifier using 90-degree hybrid couplers.

compared to the normal differential pair. This can increase the bandwidth, but at the cost of more power consumption.

2.1.7 Balanced Amplifiers

In wideband microwave amplifier design, input and output matching sections can be designed to compensate for the gain roll-off, but generally at the expense of the input and output match. The balanced amplifier solves this problem by using two 90-degree couplers to cancel input and output reflections from two identical amplifiers. The basic circuit of a balanced amplifier is shown in Fig. 2.8. The first coupler divides the input signal into two equal-amplitude components with a 90 degrees phase difference, to drive two identical amplifiers. The second coupler combines the output signals from two amplifiers. Because of the phase properties of the hybrid coupler, reflections from the amplifier inputs cancel each other at the input to the hybrid, resulting in a good input impedance matching. Similarly, output impedance matching can be achieved by the second hybrid.

The balanced amplifier has a more complex structure than a single-stage amplifier since it needs two hybrid couplers and two separate amplifier sections, but it has a number of advantages. First, each individual amplifier stages can be optimized for gain flatness or noise figure, without concern for input and output matching. Second, reflections from two amplifiers are absorbed by the coupler terminations, improving input/output matching as well as the stability of the individual amplifiers. Third, bandwidth can be more than an octave, mainly limited by the bandwidth of the coupler. In practice, balanced amplifiers usually use Lange couplers, which are wideband and very compact.
2.2 Gain-Bandwidth Product Limit

In conventional circuit design, the bandwidth is improved by minimizing various RC products. But it only leads to a relatively narrow set of options to improve bandwidth. As an example, Fig. 2.1 shows a conventional common source amplifier providing voltage and power gain from input to its output. The corresponding small signal model of such a linear single-stage amplifier is shown in Fig. 2.9 (a). The gain of this amplifier is determined by the transistor’s transconductance $g_m$ and the effective load resistor $R$. Its bandwidth is determined by the RC time constant.

An inspection of the mathematical expression describing the transfer function characteristic of such a lumped amplifier will reveal that the gain and the bandwidth can not be increased beyond a certain limit simultaneously. Therefore, these two quantities are often considered trade-offs in the design of an amplifiers. The gain-bandwidth product of the amplifier is given by [31]

$$ GBW = \frac{g_m}{2\pi C} \quad (2.8) $$
with units in hertz. As can be seen, the parasitic capacitance directly limits the bandwidth by reducing the output impedance of the amplifier as the frequency increases. Thus, maintaining a uniform output impedance over a wider frequency range will increase the GBW.

In general, the load can be treated as a network \( Z(j\omega) \), as shown in Fig. 2.9 (b). To extend the amplifier bandwidth, \( Z(j\omega) \) is expected to be a constant resistor over as wide frequency range as possible. However, there is an upper bound for such a frequency range [32]. This theoretical limit (a.k.a the Bode-Fano Limit) for the amplifier in Fig. 2.9 (b) is

\[
GBW_{\text{max}} = \frac{g_m}{\pi \overline{C}}
\]  

(2.9)

where \( \overline{C} \) is defined as

\[
\overline{C} = \lim_{\omega \to \infty} \left( \frac{1}{j\omega Z} \right)
\]

and \( Z(j\omega) \) is an impedance function. This theoretical limit means it is possible to introduce a more elaborate passive load to improve GBW, but there is always an upper bound. On the other hand, according to the feedback control theory, the gain-bandwidth product of an amplifier does not change with the presence of negative feedback. So the gain-bandwidth design tradeoff always exists.

### 2.3 Distributed Circuits and Systems

#### 2.3.1 Distributed Amplifiers

To avoid the gain-bandwidth tradeoff in the design, the distributed amplification concept was introduced, which can achieve a gain-for-delay tradeoff without affecting bandwidth [33].

The basic structure of a distributed amplifier is shown in Fig. 2.10. It has multiple gain cells connected between two transmission lines. The input transmission line connected to the gate of each transistor is called gate-line. The output transmission line connected to the drain of each transistor is called drain-line. The input signal travels along the gate-line and is tapped by each gain cell in sequence (from left to
right in Fig. 2.10). The tapped signal is amplified by the gain cell. On the drain-line, the output signals from each gain cell travel in the forward direction will sum in time coherence if the delays of the gate-line and drain-line are matched [34, 35].

Assuming the loaded gate-line and drain-line both have an impedance of \( Z_0 \), and all loss factors are ignored, the overall voltage gain is

\[
A_V = \frac{ng_mZ_0}{2}
\]

(2.11)

where \( n \) is the number of gain cells in a distributed amplifier. As can be seen from this expression, this amplifier has an overall gain that depends linearly on the number of gain cells and can operate at frequencies where each stage actually has a gain smaller than unity. Consequently, distributed amplifiers can operate at substantially higher frequencies than conventional amplifiers. It can also be observed that this distributed amplifier does trade gain for delay since the delay is also proportional to the number of stages. The bandwidth does not factor into the tradeoff in any direct way [36].

One source of bandwidth limitation in conventional amplifiers is the drop of input/output impedance with increasing frequency. However, in a distributed amplifier, the input capacitance and output capacitance of each gain cell are absorbed into the transmission line structure. Therefore, the amplifier bandwidth is determined by the capacitively loaded transmission line only. Since the input capacitances of the gain
Figure 2.11: A generic distributed architecture.

Figure 2.12: Distributed circuits expand the design space by introducing circuit complexity as a parameter.

cells are usually larger than the output capacitances, some extra capacitors need to be added to the drain-line to maintain the matched delay.
2.3.2 Distributed Architectures

Fig. 2.11 shows the concept of distributed circuits and systems on the architecture level. In general, a distributed system usually includes two major parts: multiple function blocks and the networks connecting these function blocks. Multiple function blocks are used to implement certain functions through parallel signal paths. Networks are needed to manage these function blocks so that they can work cooperatively to perform a single task. As in Fig. 2.11, the distribution network and combining network are employed to achieve the cooperation between function blocks.

From the circuit design point of view, distributed circuits essentially expand the design space by introducing the circuit complexity as a design parameter, as shown in Fig. 2.12. So it can be traded for gain, voltage swing, speed, power consumption and linearity. This is especially suitable for implementations in CMOS technologies because of the large integration capability provided.
Chapter 3

Distributed Pulse Filtering Circuits

In this chapter, distributed amplifiers (DAs) with non-uniform filtering structures and distributed transversal filters (DTFs) were developed using distributed circuit technique for the filtering of ultra-wideband pulses. New concept of network synthesis is introduced into the DA design for frequency response control. The pulse filtering capability and detailed transfer function analysis are carried on for the DTF. Binary-weighted gain cell design is also applied into the DTF design for the dynamic range enhancement. Measurement results from DA and DTF prototypes in 0.18μm digital CMOS technology successfully demonstrate the design techniques.

3.1 Introduction

Ultra-wideband pulse filtering is an important function in wireline communications, high-speed instrumentation, and radar systems for pre-emphasis, equalization, and general signal conditioning. For example, pulse filtering with multi-GHz bandwidth is required to tailor the laser drive pulse to a wide variety of target waveforms in our OMEGA laser system for inertial-confined fusion experiments [25]. In UWB impulse radios (IR-UWB), low repetition-rate, ultra-short pulses are used to
achieve lower power consumption and simpler transceiver architecture than conventional narrow-band RF systems [37]. It is challenging to generate UWB pulses that satisfy the FCC emission mask and narrow-band interference requirements. Therefore, pulse generation and filtering circuits become the critical building blocks in IR-UWB transmitter design.

Rapid progress in wideband communications, such as UWB and fiber-optic systems, are driving demands for front-end amplifiers with multi-gigahertz bandwidth. Distributed amplifiers (DAs) have always been one of the top choices for wideband amplification [38, 39, 40, 36, 41, 42]. Recently, advances in silicon technologies make it possible to build fully-integrated CMOS DAs with multi-GHz bandwidth [43, 44, 45, 46, 47], which are very attractive because of silicon’s low cost and integration capability with baseband circuits.

Not surprisingly, most of these research efforts focus on achieving large bandwidth, which means that the design usually addresses only the passband characteristics of DA’s frequency response [48, 49]. On the other hand, wideband systems increasingly require good out-of-band spectrum control to reject interference and reduce noise. For example, in IR-UWB systems, there are very stringent requirements on the signal spectrum due to concerns of interference with existing wireless services [23]. Therefore, tighter control over the overall DA frequency response is needed, and good stop-band characteristic is highly desirable. This is particularly important for CMOS DAs since they tend to have a slow slope in the stop-band due to the lossy on-chip transmission lines.

DA has been widely used as a wideband circuit topology. In order to realize UWB pulse filtering based on DA topology, we need to introduce filtering functions into it. From the basic analysis of DA, there are two important issues. First, DA’s bandwidth is determined by the uniformly loaded transmission lines. Second, the output signals from each tap are combined coherently in the forward direction on the drain line.

Considering the first issue, filtering structures can be implemented by making the loaded transmission lines non-uniform, which are synthesized according to the target responses. This idea leads to the work on distributed amplifiers with non-uniform filtering structures, which essentially utilize the passive network available inside the
conventional DAs to realize certain filtering functions. Thus, the frequency response of DAs can be well controlled by network synthesis method in filter design.

However, the determined frequency response of DAs has very limited reconfigurability since passive networks are difficult to tune after fabrication. Considering the second issue of DA design, filtering functions can be realized by combining signals in a non-coherent way. This leads to the idea of using distributed transversal filters (DTF) for pulse filtering. In this case, DA is designed to work in the reverse-gain mode, which is essentially a wideband analog finite impulse response (FIR) filter. The frequency responses are determined by the gain of each tap in the DA and the amount of delay between neighboring taps. Thus, the frequency response can be adaptively changed by tuning the gain of each tap.

### 3.2 Distributed Amplifiers with Non-Uniform Filtering Structures

This section will demonstrate a new design concept for DAs: by synthesizing the (artificial) transmission lines as non-uniform filters with specific frequency response, the DA’s spectrum can be controlled not only within the pass-band, but also in the stop-band.
Figure 3.2: The proposed DA with non-uniform filtering (bias not shown).

Figure 3.3: Model of a generic DA with non-uniform filtering structures, showing the i-th tap. For simplicity, gate and drain lines are assumed to be identical.
Figure 3.4: Comparison of DAs with different filtering functions (simulated): (a) magnitude response (b) phase response.
3.2.1 Non-Uniform Filtering

Conventional DAs usually use constant-k sections as the basic iterative structures in the gate and drain lines, and hence the latter becomes uniform (artificial) transmission lines (Fig. 3.1). M-derived sections are usually used at terminations to improve matching. Although widely adopted, constant-k sections are only one of the possible filtering structures in distributed amplifiers. The necessary condition for distributed amplification is that the signals traveling in the forward direction add in-phase and those traveling in the reverse direction are absorbed by terminations. Therefore, non-uniform filtering structures may also be used for transmission lines in the DA design, as shown in Fig. 3.2.

Can the phase synchronization be maintained if we use a non-uniform filtering structure in a distributed amplifier? To answer this question, we analyze a DA with lossless non-uniform filtering structures, and ideal transistors (unilateral and no parasitic resistance), as shown in Fig. 3.3. We are concerned only about the signal flowing through the i-th tap, and hence only its gate-line voltage and transconductance are shown. The other parts of gate and drains lines are separated into the left block $L_i$ and right block $R_i$. We define the impedance looking into the two directions as $Z_{Li}$ and $Z_{Ri}$. The voltage transfer from gate line to drain line at this tap is

$$\frac{v_{di}}{v_{gi}} = \frac{g_m}{Y_{Li} + Y_{Ri}}$$

(3.1)

where $Y_{Li} = 1/Z_{Li}$, $Y_{Ri} = 1/Z_{Ri}$, and $g_m$ is the transistor transconductance. Signals on gate line and drain line are in synchronization if the right-hand side of Eqn. (3.1) is a real number, i.e.,

$$Im\{Y_{Li}\} + Im\{Y_{Ri}\} = 0$$

(3.2)

It can be shown [50] that for a lossless passive network split into two parts like in Fig. 3.3,

$$\left|\frac{Z^*_{Li} - Z_{Ri}}{Z_{Li} + Z_{Ri}}\right| = |\Gamma_1| = |\Gamma_2|$$

(3.3)

When $\Gamma_1 = \Gamma_2 = 0$, $Z^*_{Li} = Z_{Ri}$ or $Y^*_{Li} = Y_{Ri}$. Therefore, the synchronization requirement is satisfied within the passband, given that both transmission lines are
Figure 3.5: Normalized design parameters for both filtering structures implemented as LC artificial transmission lines.

matched at terminations ($\Gamma_1 = \Gamma_2 = 0$). Note that the phase synchronization condition (Eq. (3.2)) implies maximum power transfer in the pass-band, but is generally not satisfied in the stop-band, which usually helps the stop-band performance.

In the prototypes we report below, the filtering structures of the gate-line and drain-line are constructed as Butterworth and Chebyshev functions since both are common low-pass filters used in microwave applications. It is expected that given the same bandwidth, the Butterworth one is quite close to the conventional constant-k case, with flat response within the pass-band, while the Chebyshev one shows faster roll-off in the stop-band, but its phase response is less linear (Fig. 3.4).

### 3.2.2 Circuit Design

We chose three-stage designs for the prototype DAs, which are typical for CMOS DAs. So the order of corresponding filters is determined to be seven. Network synthesis method [50] is used to generate the initial design. The normalized design parameters of LC ladder structure, beginning with a series element, for low-pass Butterworth and Chebyshev filtering, are shown in Fig.3.5 [50]. The real inductance and
capacitance values can be scaled from the normalized filter parameters:

\[ L_k = \frac{Z_0 g_k}{\omega_c} \]  
\[ C_k = \frac{g_k}{Z_0 \omega_c} \]  

where \( L_k, C_k \) are the physical inductance and capacitance values in the ladder structure, \( Z_0 \) is the characteristic impedance, \( \omega_c \) is the cut-off frequency, and \( g_k \) is the normalized design parameter in Fig. 3.5.

The schematic of prototype DAs is shown in Fig. 3.6. The cut-off frequency \( f_c = \frac{\omega_c}{2\pi} \) of both gate and drain lines is specified to be 10 GHz. The characteristic impedance (\( Z_0 \)) of both gate and drain lines is 50 \( \Omega \). In this schematic, inductors \( L'_k = L_k \), while on the gate line the input capacitance of each gain cell is designed to be \( C_k \). On the drain line, extra shunt capacitors \( C'_k \) are added with output capacitance of each stage to form \( C_k \). The inductance and capacitance values for Butterworth and Chebyshev filtering are listed in the inset table of Fig. 3.6.

Cascade configuration is chosen for the gain cell because of its large output impedance and wideband frequency response. A cascode current mirror provides dc bias. \( L_b \) and the \( C_b \) represent the bias tees and dc blocks in the test set-up. Off-chip wideband 50 \( \Omega \) terminations are used in the measurement.
The inductors are initially designed using Asitic to optimize for Q. Then the area of inductors is minimized to reduce the parasitic capacitance, which is important to maintain the constant inductance value within the pass-band. Then the complete gate and drain lines are simulated in Sonnet to generate wideband s-parameters for circuit simulation.

3.2.3 Measurement Results

The prototype DAs were fabricated using National Semiconductor’s 0.18μm digital CMOS technology with bulk silicon substrate. Spiral inductors are constructed using...
Figure 3.8: Measured performance of the prototype Butterworth DA: (a) power gain; (b) phase response; (c) input return loss; (d) output return loss.
Figure 3.9: Measured performance of the prototype Chebyshev DA: (a) power gain; (b) phase response; (c) input return loss; (d) output return loss.
Figure 3.10: Input IP3 and 1dB compression point of the prototype DAs.
the 2µm thick bump metal layer. The design rule on this metal layer results in low self-resonance frequency for the spiral inductors, and hence limits the achievable bandwidth of the prototype DAs. The chip photos are shown in Fig. 3.7. The chip size is 1.6 mm × 0.9 mm for the Butterworth one, and 1.8 mm × 1.1 mm for the Chebyshev one. The power supply is 1.5 V for both DAs. The power consumption is 51 mW and 54 mW for the Butterworth and Chebyshev DAs, respectively.

The frequency responses of both DA chips were measured via on-wafer probing. Due to the inaccuracy of on-chip capacitors and the modeling of inductor loss, there is a sloping response below 2 GHz. The gain of the Butterworth DA is 11.7 dB±0.6 dB from 2.5 GHz to 9 GHz, as shown in Fig. 3.8. The input return loss is better than −17 dB within 8.5 GHz, and the output return loss is better than −14 dB within 9.3 GHz. The small signal gain of the Chebyshev DA is 10 dB±1.0 dB from 2.5 GHz to 8.5 GHz, as shown in Fig. 3.9. The input return loss is better than −11 dB within 9.6 GHz, and the output return loss is better than −10 dB within 8.6 GHz. The transition rate to the stop-band is −5 dB/GHz for the Butterworth DA and −8 dB/GHz for the Chebyshev DA. It can be seen that both prototypes match the simulation very well.

The nonlinearity performance of the DAs is also characterized (Fig. 3.10 (a)). The input IP3 (third order intercept point) of the Butterworth DA is better than 4.5 dBm from 2 GHz to 7 GHz. The Chebyshev one is better than 5 dBm from 1 GHz to 8 GHz. The Measured 1dB compression point values are shown in Fig. 3.10 (b).

### 3.3 Distributed Transversal Filters

The goal of this study is to implement the pulse filtering function using a reconfigurable distributed transversal filter (DTF) in standard digital CMOS technologies. In Section 2.2, the DTF architecture is explained. The DTFs’ pulse filtering capability is analyzed in Section 2.3 based on the transfer function. Two circuit prototypes are presented afterwards as design examples for pulse filtering in laser systems and IR-UWB respectively.
3.3.1 DTF Architecture

In a finite impulse response (FIR) transversal filter (Fig. 3.11), the input signal \( x(t) \) propagates along a delay line. \( x(t) \) and its delayed versions \( x(t - i\tau) \) (where \( \tau \) is the unit delay, and \( i = 1, ..., N \)) are tapped along the delay line, multiplied with the coefficients \( (c_i, i = 0, ..., N) \), and then summed to generate the filtered output \( y(t) \). This architecture is usually referred as tapped-delay-line structure. A DTF [51, 52, 53] is essentially an analog FIR filter based on distributed circuit techniques, which are widely used in microwave, fiber-optical and radar systems. Fig. 3.12 shows the basic structure of an DTF, which consists of two transmission lines and multiple gain cells coupled between them. It can be viewed as a distributed amplifier [38] operating in the reverse-gain mode, and therefore inherits the latter’s unique wideband characteristics: the parasitic capacitance of transistors is absorbed into the loaded transmissions to form low-pass filtering structures. The circuit bandwidth is thus limited only by the cut-off frequency of the loaded transmission lines, and can be (by design) much larger.
than what is achievable by a lumped circuit.

Similar to a generic transversal filter, the input signal in a DTF travels along the input transmission line (gate-line), and is tapped by each gain cell in sequence (from left to right in Fig. 3.12). The tapped signal is amplified by a variable gain, which corresponds to the filter coefficient (see below). Then the output signals from all cells are power-combined on the output transmission line (drain-line) and travel to the output (from right to left in Fig. 3.12). The input signal on the gate-line is eventually absorbed by the matched termination, and so are the signals traveling to the right on the drain-line. In this architecture, the loaded transmission lines serve both as signal distribution/combining networks and delay elements. The transfer function of a DTF can be described in the time domain as

$$y(t) = \sum_{i=0}^{N} c_i x(t - \sum_{k=0}^{i-1} (\tau_{gk} + \tau_{dk}))$$  \hspace{1cm} (3.6)

where \(c_i\) is the tap coefficient and assumed to be real in a DTF. \(\tau_{gk}, \tau_{dk}\) the tap delay from the gate- and drain-line. Note that the delay between adjacent cells consists of that from both transmission lines, i.e., \(\tau_k = \tau_{gk} + \tau_{dk}\). Correspondingly, the frequency response is given by

$$H(j\omega) = \sum_{i=0}^{N} c_i \exp(-j\omega \sum_{k=0}^{i-1} \tau_i)$$  \hspace{1cm} (3.7)

For a typical DTF with uniform distributed gain cells, \(\tau_k = \tau\)

$$H(j\omega) = \sum_{i=0}^{N} c_i \exp(-ji\omega\tau)$$  \hspace{1cm} (3.8)

Apparently, the tap delay \(\tau\) sets the sampling frequency of an DTF, and hence imposes another constraint on its frequency response in addition to the cut-off frequency of the loaded transmission lines. \(\tau\) is determined by the transmission lines design, and can be as small as tens of picoseconds using current integrated circuit technologies (see Section IV below), which corresponds to multi-gigahertz bandwidth for the filter. The cut-off frequency tends to be higher than the sampling frequency. Therefore, an
integrated DTF can be used in IR-UWB systems for pulse filtering and interference suppression.

An integrated DTF has some distinctive advantages: 1) it can achieve much larger bandwidth with relatively low power consumption compared to a digital FIR filter. The latter has to be implemented in ultra-high-speed digital circuits, which consume comparable if not more power than a DTF, not to mention (again) the ultra-high-speed ADC needed to sample and quantize the pulse. 2) Compared to other analog transversal filters, transmission lines can be easily implemented on-chip, while CCD or SAW devices cannot. 3) The filter coefficients can be easily and independently controlled by gain cells, and thus it is inherently reconfigurable.

3.3.2 Pulse Filtering Analysis

In order to generate target spectrum of UWB signals or suppress the narrow-band interference (NBI), a DTF needs to be synthesized for specific transfer functions in frequency domain. In general, the transfer function of a DTF is expressed as Eq. 3.7. If we assume the delay between adjacent cells are identical, as in Eq. 3.8, the transfer function of a DTF can be expressed as the truncated Fourier expansion. Therefore, the basic design goal is to determine all the coefficients $c_k$ so that the synthesized function $H(j\omega)$ is the best approximation for a target response function [54]. Let $G(j\omega)$ to be a prescribed target transfer function and only the magnitude response matters. The phase response is assumed to be linear which implies the coefficients distribution must exhibit symmetry relative to the center of the DTF.

Under the linear phase assumption, the coefficients can be determined as

$$c_i = \frac{1}{\omega_2 - \omega_1} \int_{\omega_1}^{\omega_2} |G(j\omega)| \exp(jk\omega T) d\omega,$$

(3.9)

where $i = 0,1,...,N/2$, $\omega_1$ and $\omega_2$ are the lower and upper bounds of the target frequency band, respectively, beyond which the magnitude of $G(j\omega)$ is considered to be zero. Due to the symmetry of coefficients, $c_i = c_{N-i}$ for $i = N/2 + 1,...,N$. 
Figure 3.13: (a) LC line ladder structure; (b) generic ladder structure.

Figure 3.14: Ladder structure for the drain line.

3.3.3 Circuit Level Transfer Functions of DTF

The overall transfer function of DTF is determined by the transfer function of each tap, mostly determined by the LC ladder structure, as in Fig. 3.13 (a). The transfer functions in the LC ladder structure can be derived based on the iterative analysis of the generic ladder structure. The generic ladder structure is shown in Fig. 3.13 (b). In such a structure, each series branch is characterized by its impedance and the current flowing through the branch, and each shunt branch is characterized by its admittance and the voltage drop on that branch.
Starting from the right end of the ladder structure,

\[ A_{n+1} = \frac{V_{n+1}}{V_{n+1}} = 1 \]  \hspace{1cm} (3.10)

\[ S_{n+1} = \frac{I_{n+1}}{V_{n+1}} = Y_{n+1} \cdot A_{n+1} \]  \hspace{1cm} (3.11)

For \( i = 1 \) to \( n \), we have

\[ A_i = \frac{V_i}{V_{n+1}} = Z_{i+1} \cdot S_{i+1} + A_{i+1} \]  \hspace{1cm} (3.12)

and

\[ S_i = \frac{I_i}{V_{n+1}} = Y_i \cdot A_i + S_{i+1} \]  \hspace{1cm} (3.13)

when \( i \) is odd.

If the voltage source \( V_0 \) is used as the reference, the voltage transfer function to each shunt branch is

\[ H_i = \frac{A_i}{A_0} \]  \hspace{1cm} (3.14)

where \( i \) is from 1 to \( n \).

The frequency response of each tap in DTF can be expressed as series connected three blocks, gate-line, gain cell and drain-line, i.e.

\[ H_i = H_{g,i} \cdot H_{g,c,i} \cdot H_{d,i} \]  \hspace{1cm} (3.15)

The transfer function on the gate-line for tap \( i \) is

\[ H_{g,i} = \frac{A_i}{A_0} \]  \hspace{1cm} (3.16)

The transfer function on the drain-line for tap \( i \) can be analyzed using Fig. 3.14. It is assumed that the drain-line and the gate-line are identical and the ladder structure is symmetric.

\[ Y_{i,i} = \frac{S_{n-i+1}}{A_{n-i}} \]  \hspace{1cm} (3.17)
\[ Y_{r,i} = \frac{S_{i+1}}{A_i} \]  

(3.18)

The gain cell is modeled as a voltage-controlled current source with a transconductance \( g_{m,i} \). Such a simplified model is valid within a wide bandwidth since the frequency dependence of each gain cell is caused by the input/output capacitance. So the transfer function of the gain cell

\[ H_{g,i} = g_{m,i} \]  

(3.19)

The voltage generated by the current source \( g_{m,i}V_{g,i} \) is

\[ V_{d,i} = \frac{g_{m,i}V_{g,i}}{Y_{l,i} + Y_i + Y_{r,i}} \]  

(3.20)

Thus, the voltage on the load is

\[ V_{a,i} = \frac{V_{d,i}}{A_{n-i}} \]  

(3.21)

By combining Eq. 3.16, Eq. 3.19, Eq. 3.20 and Eq. 3.21, we can get the transfer function on the drain line.

\[ H_{d,i} = \frac{1}{(\frac{A_{n-i+1}}{A_{n-n}} + Y_i + \frac{A_{i+1}}{A_i}) \cdot A_{n-i}} \]  

(3.22)

Therefore, the transfer function of each tap in DTF is

\[ H_i = \frac{A_i}{A_0} \cdot g_{m,i} \cdot \frac{1}{(\frac{A_{n-i+1}}{A_{n-i}} + Y_i + \frac{A_{i+1}}{A_i}) \cdot A_{n-i}} \]  

(3.23)

The overall transfer function of the DTF is

\[ H = \sum_{i=1}^{n/2-1} H_{2i} \]  

(3.24)
3.3.4 Noise Analysis

In the practical implementation of DTF, there are many noise sources, such as power lines, substrates and so on. The noise will cause the filter coefficients and tap delay deviated from their ideal values. The effects of the noise on the DTF performance are analyzed here.

The coefficients of DTF become $c_i + e_i$ with the random error $e_i$ caused by the noise.

$$y(t) = \sum_{i=0}^{N} (c_i + e_i)x(t - iT_d)$$  \hspace{1cm} (3.25)

Here $T_d$ is used to denote the tap delay to distinguish from the $\tau$ used for autocorrelation calculations. so, the transfer function is

$$|H(j\omega)|^2 = \left| \sum_{i=0}^{N} c_i e^{-j\omega iT_d} \right|^2 + \sum_{i=0}^{N} \sigma_{e_i}^2$$  \hspace{1cm} (3.26)

So, the effect of the gain noise is to offset the target transfer function by the noise power. For notch generation in the frequency domain, the transmission zeros would be offset by the noise power term, which cause the notch attenuation to be reduced.

The other effect of noise is on the tap delay. In this case, the output of the DTF is

$$y(t) = \sum_{i=0}^{N} c_i x(t - iT_d - \sum_{j=1, i \neq 0}^{i} d_j)$$  \hspace{1cm} (3.27)

where $d_j$s are independent random variables which follow the Gaussian distribution $N(0, \sigma_d^2)$. If we denote

$$D_i = \sum_{j=1, i \neq 0}^{i} d_j$$  \hspace{1cm} (3.28)

so, $D_i$ should follow $N(0, i\sigma_d^2)$.

The autocorrelation of $y(t)$ is

$$E[y(t)y(t + \tau)] = E\left[\sum_{i=0}^{N} c_i x(t - iT_d - D_i) \cdot \sum_{k=0}^{N} c_k x(t + \tau - kT_d - D_k)\right]$$  \hspace{1cm} (3.29)
For $i = k$,

$$
\sum_{i=0}^{N} E[c_i^2 x(t - iT_d - D_i)x(t + \tau - iT_d - D_i)] = \sum_{i=0}^{N} c_i^2 E[x(t)x(t + \tau)]
$$

(3.30)

So,

$$
|Y(j\omega)_{i=k}|^2 = \sum_{i=0}^{N} c_i^2 |X(j\omega)|^2
$$

(3.31)

For $i \neq k$, by taking the Fourier transform,

$$
|Y(j\omega)_{i\neq k}|^2 = \sum_{i=0}^{N} \sum_{k=0,k\neq i}^{N} c_i c_k e^{-j\omega(k-i)T_d} \exp\left(-\frac{\omega^2(i+k)\sigma_d^2}{2}\right) |X(j\omega)|^2
$$

(3.32)

So, in total, the transfer function is

$$
|H(j\omega)|^2 = \sum_{i=0}^{N} c_i^2 + \sum_{i=0}^{N} \sum_{k=0,k\neq i}^{N} c_i c_k e^{-j\omega(k-i)T_d} \exp\left(-\frac{\omega^2(i+k)\sigma_d^2}{2}\right)
$$

(3.33)

### 3.3.5 DTF Prototype for Pulse Filtering in Laser Systems

A distributed transversal filter (DTF) is a good candidate for adaptive processing of UWB pulses in laser systems. In this study, we investigate DTFs for sub-nanosecond pulse synthesis using standard CMOS technologies. A 5-tap DTF was designed using LC artificial transmission lines. A pulse synthesis algorithm was developed for DTFs. A prototype was fabricated using a standard 0.18$\mu$m digital CMOS technology. It successfully demonstrated the sub-nanosecond pulse synthesis capabilities.

### Circuit Design

The detailed schematic of a DTF is shown in Fig. 3.15-a. It consists of a number of gain cells coupled between two LC artificial transmission lines. The total delay is determined by the target pulse width, and the delay per stage is set by the pulse temporal resolution. In this design, the delay is specified as 50 ps/tap, and 200 ps in
Figure 3.15: Circuit schematics. (a) 5-tap DTF; (b) gain cell.
total, which means the number of stages is 5.

In order to achieve a large time delay like 200 ps on-chip, we choose artificial transmission lines constructed by LC ladder structures, which use less chip area compared to micro-strip lines or coplanar waveguides. The inductors are spiral inductors built with the top metal layer, and extra loading capacitors are added to achieve the required delay. The cut-off frequency of both loaded transmission lines are designed to be larger than the specified 3-dB bandwidth of the filter, which is 7GHz. Note that the cut-off frequency and delay are closely related to each other since both are determined by the loaded transmission lines. In fact, we can trade bandwidth for delay, and vice versa. Another constraint on the LC transmission lines is their characteristic impedance (Z₀). In this design, Z₀ is specified to be 50 Ω within the passband. M-derived sections are added to improve the impedance matching at both ends of the transmission lines.

The gain cell is a two-stage amplifier with internal matching (Fig. 3.15-b). The first stage is a common-source amplifier, which serves as a buffer for the second stage in order to reduce the signal attenuation on the gate-line and achieve the required bandwidth. Transistors M₂ and M₃ form a cascode amplifier, which has a relatively high output impedance, and thus good for reducing the loss on the drain line. The gain of each gain cell can be adjusted independently by tuning the bias current source of the cascode amplifier, Iᵣ, using a current mirror. In order to maintain the bandwidth, the high output impedance of the common-source buffer has to be separated from the large input capacitance of M₂. This is done by inserting an internal matching network, consisting of inductors L₁, L₂ and resistor R₁. All capacitors (C₉₁, C₉₂ and C₉₃) are by-pass capacitors.

The spiral inductors and interconnect are simulated in an electromagnetic simulator, Sonnet, to find the wideband s-parameters. Advanced design system (ADS) software is used for circuit simulation, and Cadence is used for chip layout.

**Pulse Synthesis Algorithm**

The algorithm for pulse synthesis has been developed for DTFs. In the time domain, the output waveform is a weighted sum of delayed narrow pulses generated
by each gain cell (Eq. 3.6). Since pulse amplitude can be tuned independently, the pulse responses from all taps with maximum peak amplitudes form a set of basis functions, denoted as \( b_1(t), b_2(t), \ldots, b_N(t)\). Let the target waveform be described by function \( f(t)\), and the delay per tap \( \tau\). For the first \( \tau\) seconds of \( f(t)\), only the pulse response of the first tap is available at the output. So the scaling factor for basis function \( b_1(t)\) can be easily determined by correlating the target waveform and the basis function

\[
c_1 = \frac{\langle b_1(t), f(t) \rangle}{|b_1(t)|^2} \tag{3.34}
\]

Considering that the pulse responses of adjacent taps usually overlap, a new target waveform for the remaining taps is given by

\[
f_i(t) = f(t) - b_1(t) \cdot c_1 \tag{3.35}
\]

The effect of the first tap pulse response has been subtracted from the target waveform. Similarly, the scaling factor is determined by

\[
c_2 = \frac{\langle b_2(t), f_1(t) \rangle}{|b_2(t)|^2} \tag{3.36}
\]
The remaining scaling factors can be calculated by following this procedure,

\[ f_{i-1}(t) = f_{i-2}(t) - b_{i-1}(t) \cdot c_{i-1} \quad (3.37) \]

\[ c_i = \frac{\langle b_i(t), f_{i-1}(t) \rangle}{|b_i(t)|^2} \quad (3.38) \]

After several iterations, the scaling factors \( c_1, c_2, \ldots, c_N \) for all the taps can be determined. Fig. 3.16 shows square and Gaussian pulses\(^1\) constructed using the prototype DTF in simulation. These pulses are chosen as representative ones since square waveforms are essential in wireline communications, and Gaussian pulses are widely used in IR-UWB systems. The input is an ideal Gaussian pulse with a \( T_{au} \) of 40 ps, similar to the one used in the measurement below. The synthesized square pulse has a rise time of 70 ps, and pulse width 260 ps, while Gaussian pulses have \( T_{au} \) of 60 ps and 100 ps.

**Measurement Results**

The prototype DTF was fabricated in National Semiconductor’s 0.18\( \mu \)m standard digital CMOS technology with low-resistivity substrate. The chip occupies 1.92 mm by 0.95 mm (Fig. 3.17). The power supply voltage is 2 V.

The prototype DTF is characterized in both the frequency and time domain via on-wafer probing. The frequency response of each tap is shown in Fig. 3.18. The low frequency response matches with design, while the high frequency part (>1 GHz)  

\(^1\)Gaussian pulse can be described as \( f(t) = Ae^{[t-(T_x)]/T_{au}}^2 \), where \( A \) is the amplitude and \( T_{au} \) is the pulse shape parameter.
Figure 3.18: Frequency response of each tap in the prototype DTF.

Figure 3.19: Pulse response of each tap in the prototype DTF.

Figure 3.20: Gain control linearity of each tap in the prototype DTF.
Figure 3.21: Measured waveforms synthesized using the prototype DTF. (a) square pulse; (b) Gaussian pulses.
shows larger attenuation and faster roll-off due to inaccurate modeling of loss in on-chip inductors and extra loading capacitors. Impulse response of each tap (Fig. 3.19) is measured using a Picosecond Pulse Labs 4500E pulse generator with 5210 impulse generator, which is very close to a Gaussian pulse with a $T_{\text{on}}$ of 40 ps. The tap delays are measured at the middle point of the rising edge, which are 44.6 ps, 47.3 ps, 46.7 ps, 44.1 ps. This shows a good match with the design value of 50 ps. The delays also have good uniformity for all five taps, which is an obvious advantage of integrated circuit solutions compared to discrete implementations. Because of the lossy on-chip inductors, output pulses broaden with increasing number of taps since for larger number of taps the signal needs to travel a longer distance on the LC artificial transmission lines from the input port to the output port.

The gain control of each tap is shown in Fig. 3.20, which is tuned by changing $I_c$ through a current mirror in each cell. The curves are plotted in log-log scales to better show the linearity across the dynamic range of 8-10 dB. The tuning curves show some nonlinearity for higher value bias current because of the gain saturation. This relation between pulse amplitude and bias current is then used in the pulse synthesis to correct this nonlinear effect.

Some example waveforms are constructed in measurement using our pulse synthesis algorithm, as shown in Fig. 3.21. The filter can adequately synthesize a square waveform with 80 ps rise time and 380 ps pulse width (FWHM) in Fig. 3.21-a. The total power consumption in this case is 95 mW. In Fig. 3.21-b, the synthesized Gaussian pulse has a $T_{\text{on}}$ of 75 ps. Here the filter consumes 84 mW. Both are quite close to the simulation results shown above. The Gaussian pulse has a lumpy tail which comes from both the input pulse tail and the termination reflections.

### 3.3.6 DTF prototype for Pulse Filtering in IR-UWB Systems

In recent years, RF integrated circuits operating at low GHz range have been gradually migrated to low-cost digital CMOS technologies, and the trend is continuing for microwave and even millimeter-wave integrated circuits at 10 GHz and beyond [55][56] [57]. It is commonly believed that this transition only degrades the
performance of RF circuits except in terms of cost. For example, the low supply voltage in the deep-submicron process (1.5V or lower) and relatively high threshold voltage (0.5V or higher) severely limits the voltage headroom and dynamic range of RF circuits [11]. The thin metals and lossy silicon substrate significantly lower the quality factor (Q-factor) and self-resonant frequency of on-chip inductors and transmission lines. Therefore special RF CMOS processes have been developed to mitigate the performance degradation at extra cost. What is usually untapped is the benefit of large-scale integration in digital CMOS technologies, which were not feasible for conventional RF IC designs in III-V technologies. In fact, circuit complexity can be traded for speed, power and/or accuracy. Digital CMOS technologies enable us to digitally control RF circuits, and further to integrate analogy/digital signal processing techniques with RF designs. This approach also improves scalability and reconfigurability of RF circuits, which is crucial for future multi-mode, multi-standard, frequency-agile radios. Digitally-assisted RF circuits will more be likely to benefit instead of suffering when CMOS technologies advance.

In this section, we introduce binary-weighted digital control into the gain cell design of a distributed transversal filter (DTF) to demonstrate the benefits of digitally-assisted RF circuits. By effectively integrating a digital-to-analog converter (DAC) into the gain cell, the new design can improve gain cell’s linearity and hence DTF’s dynamic range. A 5-tap DTF prototype was designed and implemented in a standard 0.18μm digital CMOS technology, using LC artificial transmission lines with on-chip spiral inductors, and gain cells with a quasi-differential amplifier design. 3-bit digital control and analog tuning are both implemented for gain control in each gain cell. The new design achieves a dynamic range of 13 dB. UWB waveforms are generated using the DTF prototype.

**Gain Control: Analog vs. Digital**

For most DTF applications, it is highly desirable to control the filter coefficients linearly, which are represented by the gain of embedded amplifiers (gain cells). In particular, when a DTF is used for pulse synthesis, the amplitude linearity of gain control determines the DTF’s dynamic range for a given input pulse. A second challenge of
a linearly-controlled DTF is to maintain the pulse shape across the dynamic range. This means that only the magnitude frequency response of a DTF ($|S_{21}|$) changes linearly with the control signal, and its phase response ($\angle S_{21}$) and return loss ($S_{11}$ and $S_{22}$) remain unchanged. The latter cannot be ignored because it tends to vary with frequency and hence is difficult to achieve perfect impedance matching throughout the wide bandwidth. In previously reported DTFs, gain control is accomplished by analog means, usually varying the bias condition of gain cells, e.g., by tuning the bias current [58, 59]. These analog gain control mechanisms are easy to implement since they are already part of the gain cell design. However, the achievable dynamic range is severely limited (less than 8 dB in reports) due to the fact that the bias condition cannot be changed significantly without disrupting the circuit operation. When the bias is tuned, the parasitic capacitance of transistors and impedance level at critical nodes change, and so is the phase response, which usually degrades when the bias condition deviates from the optimum.

In order to maintain the phase response of a DTF, the bias tuning range needs to be minimized so that the parasitic capacitance of each gain cell and the impedance level at each node of the signal path change little. In order to improve the return loss, the loading of gain cells on both transmission lines (particularly the gate line) should remain constant when tuning the gain. Both requirements dictate a new gain control mechanism in addition to the analog tuning. A digital gain control method is highly desirable since it provides a direct interface for digital signal processing at baseband.
Another advantage is a possible coarse-fine dual control mechanism: digital control for coarse tuning, and analog control for fine tuning.

To implement the digital control, a gain cell can be constructed using multiple amplifiers connected in parallel instead of a single amplifier. Digital gain control is accomplished by turning on/off the right amplifiers. Essentially, we integrate a digital-to-analog converter (DAC) into the gain cell. A DTF with both the digital and analog gain control is shown in Fig. 3.22. In this case, the analog tuning only needs to cover the range between neighboring two discrete levels set by the digital control which is \(2^N - 1\) smaller than the conventional analog tuning, where \(N\) is the number of bits for digital control.

**Circuit Design**

A prototype 5-tap DTF is implemented as shown in Fig. 3.22. It consists of 5 gain cells connected in parallel between two LC artificial transmission lines. Each gain cell includes a number of amplifiers. In order to achieve the best gain-control linearity, each amplifier (called unit cell) in the gain cell is designed to be identical, and the binary-weighted digital control bits are connected to the corresponding number of unit cells. For example, a 3-bit digital-controlled gain cell is constructed with 7 unit cells, with each bit controls 1, 2, and 4 unit cells, respectively, so that 8 discrete gain levels can be generated, as shown in (Fig. 3.23 (a)).

The unit cell is implemented using a current-steering structure [58] as shown in Fig. 3.23 (b). Here a quasi-differential amplifier is used to generate pulses with both polarities without the overhead in chip area and difficulty in wideband differential measurement. The cascode transistors \(M_3 - M_6\) are used to steer the output current between the output and dummy terminals. They are controlled by \(V_{pos}\) and \(V_{neg}\), which are determined by the digital control bits and pulse polarity as shown in the inset table in Fig. 3.23 (b). Note that the current through the input transistor \(M_1\) remains unchanged no matter which path the output current is steered to. Therefore, digital control does not affect either the bias condition of the analog part of the gain cell, or the capacitive loading on the transmission lines. The latter is important
Figure 3.23: (a) Binary-weighted gain cell, each digital bit controls a number of identical unit cells. (b) Each unit cell is implemented as a current-steered quasi-differential amplifier with tail current tuning.
to maintain both the phase response and insertion loss. Analog gain control is implemented by tuning the tail current source. Since it is used to fill the gain values between the discrete digitally-controlled gain levels, only the unit cell corresponding to the least-significant-bit (LSB) needs to be tuned.

The DTF delay is specified as 50 ps/tap, and 200 ps in total. The 50 ps/tap corresponds to 20 GHz sampling frequency which is needed to synthesize the frequency spectrum within 10 GHz. The characteristic impedance $Z_0$ of both gain-line and drain-line is specified to be 50 $\Omega$ within the passband. The prototype DTF was fabricated in a standard 0.18 $\mu$m digital CMOS technology with low-resistivity substrate. The chip size is 3.16 $mm$ by 1.46 $mm$ (Fig. 3.24).

**Measurement Results**

The frequency responses of each tap are shown in Fig. 3.25. The bandwidth of tap1 is about 14 GHz and decreases for other taps because as signal travels a longer distance. The sloping response below 2 GHz is caused by the resistance loss on the LC lines. The phase responses are quite linear within 9 GHz for all five taps. The digital gain control is demonstrated in Fig. 3.26 (a) using tap1 as an example. The magnitude response $|S_{21}|$ changes linearly with the digital control signal. The phase responses and input return loss $S_{11}$ show little change for different digital gain levels (Fig. 3.26 (b), (c)), which verifies that the RF performance is well conserved using digital gain control.
Figure 3.25: Measured frequency responses of each tap.

Time-domain impulse response characterization of the prototype DTF is performed using an input pulse with 80 ps pulse width from an impulse generator. The impulse response of each tap is shown in Fig. 3.27, from which the delay uniformity for all five taps can be observed. The gain control of each tap is shown in Fig. 3.28. In Fig. 3.28 (a), for total bias current between 0.75 mA and 5.25 mA, the digital control shows very good linearity. The tail current tuning of the quasi-differential amplifier is shown in Fig. 3.28 (a) for total bias current lower than 0.75 mA and larger than 5.25 mA. Some nonlinearity occurs within these ranges because of the gain saturation and the parasitic capacitance change. The pulse shape change with tuning signal can be quantified by the correlation factor as shown in Fig. 3.28 (b), in which the output pulse at 5.25 mA bias current is selected as the reference. Within the dynamic range of about 13 dB, the correlation factor is more than 0.9. The analog tuning provides about 5 dB dynamic range and the digital control provides about 8 dB additional dynamic range.

Some UWB waveforms generated using the prototype DTF are shown in Fig. 3.29 with corresponding spectra. The DTF is driven by an input impulse train running at 500 MHz. Fig. 3.29 (a) (b) show the waveform and spectrum generated using 2 taps. Fig. 3.29 (c) (d) show the waveform and spectrum generated using 5 taps. The signal power distribution is pushed to higher frequency by using more taps. Since
Figure 3.26: Measured frequency responses of tap1 with digital control.
Figure 3.27: Impulse response of each tap in the prototype DTF. The interstage delay is 48.6 ps, 49.9 ps, 51.5 ps, 50.5 ps.

Figure 3.28: Tuning of each tap in the prototype DTF: (a) Pulse amplitude; (b) Correlation factor.
Figure 3.29: Generated UWB waveforms and spectra using the prototype DTF
the bandwidth of last three taps can not cover up to 10 GHz, the spectrum at the high frequency end (>5 GHz) is only shaped by the first two taps. But for the spectrum at low frequency end (<3 GHz), it is shaped by all five taps. That is why the generated UWB spectra can still have power distribution at frequencies higher than the bandwidth of last three taps in the DTF.

### 3.3.7 DTF Performance Limitations

The DTF provide a wideband filter solution for UWB pulse processing. However it suffers from the inherent delay-bandwidth tradeoff. As shown in Fig. 3.30, in DTF the gate-line is used to distributed input signal to each gain cell and the drain-line combines output signals from each gain cell. The timing control function is essentially realized using the gate-line and drain-line, as described in

\[
\tau = \sqrt{LC}
\]  

(3.39)

where \( L \) and \( C \) are the inductance and capacitance values used to form the LC artificial transmission line. At the same time, the gate-line and drain-line are also required to have large signal bandwidth since they are used for the distribution and combining of wideband signals. The bandwidth can be calculated using

\[
f_c = \frac{1}{\pi \sqrt{LC}}
\]  

(3.40)
Thus, due to the fact that two functions, timing control and wideband signal combining, are implemented using the same passive transmission lines, a direct tradeoff exists between the tap delay and bandwidth, as shown in the equation below.

\[ f_c \cdot \tau = \frac{1}{\pi} \quad (3.41) \]

This relation basically means if longer pulse duration needs to be synthesized for a certain number of taps, then the tap delay needs to increase, but it will cause the reduction of bandwidth. The way to address this is to implement timing control and wideband signal combining using different function blocks, which will be discussed in the next chapter.

The DTF has very limited delay tuning capability because of passive LC artificial transmission lines. The bandwidth of DTFs is also mostly limited by the lossy LC lines, which significantly degrade the performance of DTFs.

### 3.4 Summary

In this chapter, distributed amplifier with non-uniform filtering structures and distributed transversal filter (DTF) were proposed to implement the wideband pulse filtering functions.

We demonstrated that non-uniform filtering structures can be used in DAs for better control of the frequency response in both pass-band and stop-band. Prototype DAs with Butterworth and Chebyshev filtering designed and implemented using a 0.18\(\mu\)m digital CMOS technology. Measurement results verified the new design concept.

A 5-tap DTF was designed using a 0.18\(\mu\)m standard digital CMOS technology with 50ps time resolution. The time-domain measurement results demonstrate its capability in sub-nanosecond pulse synthesis, potentially for pulse filtering applications in OMEGA laser system.

A 5-tap DTF with a new gain cell design was implemented based on the design concept of digitally-assisted RF circuits. The gain cell is a quasi-differential amplifier
with both 3-bit digital control and analog tuning. Measurement results demonstrate that such a hybrid tuning technique achieved 13 dB dynamic range. As a demonstration of its pulse filtering capability, some UWB waveforms/spectra are generated using the prototype DTF.
Chapter 4

Distributed Waveform Generators

In this chapter, the distributed architecture is applied into the generation of ultra-wideband pulses using a newly-developed circuit, distributed waveform generator (DWG), with filtering and modulation functions. The trading of circuit complexity for high-speed and low power consumption has been experimentally demonstrated using a 10-tap, 10GS/s single-polarity DWG prototype with digital pulse generators. For low-power IR-UWB applications, a 10-tap, 10GS/s, dual-polarity DWG with pulse position modulator was implemented as the transmitter with 3-9GHz bandwidth and 45pJ/pulse power efficiency. To trade circuit complexity for accuracy, digital-to-analog converters (DAC) assisted pulse generators were incorporated into a 10.9GS/s DWG prototype to achieve more than 20dB dynamic range of pulse generation. A DWG-based IR-UWB transmitter with PSM capability was also demonstrated.

4.1 Introduction

Pulse generation is a critical function in wireline communications, high speed instrumentation, and pulse radar systems. Recently, ultra-wideband (UWB) communications has emerged as one of the future generation wireless technologies, and generated new interests in high speed pulse generation and processing. Particularly, impulse radio UWB (IR-UWB) promises significantly higher data rate in low-cost, low-power wireless applications, such as wireless sensor networks, than conventional
Figure 4.1: UWB spectrum: (a) UWB band allocation with other existing wireless networks including WiMax; (b) UWB emission mask of different regions.

Narrow-band systems such as Bluetooth [60] and Zigbee [61]. For example, IR-UWB has been specified as an alternative physical layer for the low-power, low-rate wireless connectivity such as radio links in IEEE 802.15.4a standard, with a data rate up to 27.24 Mbps [23] as compared to Zigbee’s 250 kbps.

As shown in Fig. 4.1 (a), UWB band spans 7.5GHz (from 3.1 GHz to 10.6 GHz), the largest bandwidth for any commercial wireless systems. The transmit power is specified to be lower than -41.3 dBm/MHz to avoid the interference with other
existing wireless networks in the same frequency band. The challenge in building an IR-UWB system lies in two folds: (a) how to achieve the large signal bandwidth, or equivalently, how to generate and process the UWB pulses with sub-nanosecond time resolution; and (b) how to accomplish this with low power consumption and small circuit complexity, which translates into low cost. The latter requirements are particularly important for battery-powered IR-UWB systems such as wireless sensor networks. A fully integrated IR-UWB transceiver in CMOS technologies are conceived as the solution to address such conflicting requirements, thanks to CMOS’s well-known cost advantages, system-on-chip (SoC) capabilities, and aggressively improving device performance [62].

Within the 7.5 GHz bandwidth, other wireless networks also exist, e.g. 802.11a (Fig. 4.1 (a)), and hence there are stringent requirements on UWB spectrum and narrow band interference suppression. Because of the interference suppression requirements, it is critical to generate UWB pulses that are (a) compliant with regulatory power emission masks (Fig. 4.1 (b)), and (b) robust in a crowded narrow-band interference environment [37]. Both require a stringent control on the UWB pulse spectra, or equivalently, the pulse shapes.

Further, different regional regulations will require various pulse shapes or spectra, as shown in Fig. 4.1 (b), therefore a reconfigurable pulse generator, which can be tuned in situ after fabrication, is highly desirable. To achieve the best system performance, a reconfigurable UWB pulse generator is also needed to accommodate process, voltage, and temperature (PVT) variations, which has become increasingly problematic in nanoscale CMOS technologies. Such adaptive architectures are becoming more attractive as CMOS technologies further scale, and IR-UWB applications compete with more emerging wireless systems such as WiMax [63] on the spectrum usage.

Another adaptive method to improve the performance of an IR-UWB system is to use different modulation schemes according to the channel environment, type and amount of transmit data, as well as power budget [64]. For example, in a wireless sensor network, a simple modulation scheme such as pulse position modulation (PPM) can be used for a small amount of data like temperature at low data rate to save power,
while a more advanced modulation such as quadrature phase shift keying (QPSK) would be more energy efficient to transmit a larger data package like video. Variable modulation capability, therefore, is highly desirable for an IR-UWB transmitter, if it can be implemented without significant overhead in circuit complexity and power consumption.

### 4.2 Conventional UWB Pulse Generators

Currently, UWB pulse generators fall into three main categories, as shown in Fig. 4.2. One way is to generate a baseband pulse using device characteristics, and then up-convert it to the target frequency band [65, 66]. Similar to conventional narrow-band systems, this carrier-based approach circumvents the difficult task of generating wideband RF signals (UWB pulses). However, circuit complexity and power consumption of the UWB transmitter increase due to the need for a phase-locked loop (PLL) as the local oscillator (LO), and a mixer for up-conversion, both operating at multiple GHz range. Furthermore, there is a new challenge in generating baseband pulses with large bandwidth, resulting in a limited system bandwidth, typically about 2 GHz, and hence the up-converted UWB pulses can only occupy either the low band (3-5 GHz) or part of the high band (6-10 GHz). Some clever circuit techniques can be applied to simplify the architecture and reduce the power consumption, e.g., by directly switching on and off an RF oscillator using the modulated baseband data instead of up-conversion using a mixer [67]. Due to the transient time to start and stop the oscillator, however, the generated pulse width is usually quite large (more than 3 ns in [67]), and hence generated UWB pulses can only occupy a small bandwidth (528 MHz in [67]).

A second approach is to first generate a very short baseband pulse with large signal bandwidth, which generally does not meet the spectra requirement of UWB systems, and then shape it using a passive bandpass filter to satisfy the UWB emission masks [68, 69]. Again, due to the bandwidth limitation on the baseband pulse, the filtered UWB pulse usually occupies only the low-band. Further, passive filters are difficult to integrate on-chip due to the large component size. They also cause
Figure 4.2: Current IR-UWB pulse generation approaches: (a) up-conversion; (b) passive filters; (c) high-speed DAC. Both generated waveforms and pulse spectra are shown in each approach. Note that in the DAC approach, the spectrum in discrete time domain is periodic over the sampling frequency $f_s$. 
significant performance degradation due to the low quality factor ($Q$) of on-chip inductors, capacitors, and transmission lines. Therefore, these pulse shaping filters are typically implemented off-chip [70], and hence they have very limited tuning capability after fabrication. A UWB transmitter based on this architecture, therefore, can only generate a specific pulse shape, and is hardly reconfigurable.

The third approach for UWB pulse generation is waveform synthesis based on high-speed digital-to-analog converters (DAC) [71]. High speed DACs with good resolution can generate almost arbitrary pulse shapes and hence are fully reconfigurable as UWB pulse generators. A DAC-based UWB pulse generator, however, requires Nyquist rate sampling, e.g., at least 10 GS/s for the low band, and over 20 GS/s for the high band. The high sampling rate poses a challenge not only for the DAC, but also for generating the input data stream, which usually requires power-hungry high speed digital circuits using advanced technologies such as SiGe BiCMOS [71]. Therefore, it is imperative to leverage some analog and RF techniques to reduce the bandwidth and power requirement in a waveform synthesis architecture. For example, UWB pulse generation has been demonstrated using multiple edge combiner or digital switching circuits [72, 73, 74]. Although consuming relatively low power, these circuits did not achieve large bandwidth (less than 2 GHz -10 dB bandwidth in [73]), or reconfigurability, were only capable of generating a specific pulse shape (e.g. pseudo-raised-cosine pulse envelop [72]).

Since the pulse duration in IR-UWB is usually a few nanoseconds, and the pulse shape does not change in real time, a time-interleaved architecture with multiple pulse generators becomes a good solution. This led to the idea of a distributed waveform generator (DWG) [75]. Compared to those existing solutions based on waveform synthesis, DWG enables the generation of pulses with not only low power consumption, but also reconfigurable spectra and much larger signal bandwidth.
4.3 DWG for UWB Pulse Generation

4.3.1 UWB Pulse Characteristics

As shown in Fig. 4.3, there are several distinctive features of UWB pulses: (a) They have very short duration, less than 1 ns when the full 7.5 GHz bandwidth is utilized, or only 2 ns for the low band. (b) The large bandwidth translates into a fine time resolution, which requires a Nyquist sampling rate as high as 20 GSamples/s for the full band, and 10 GS/s for the low band. (c) The pulse rate $f_p = 1/T_p$ \(^1\) varies within a wide range from kHz to hundreds of MHz for different applications. (b) and (c) mean that the duty cycle of the transmit signal can be as low as 0.001\%. To save power, therefore, the pulse generator and other circuitry in the transmitter should operate only when a pulse is transmitted, i.e., they should be duty cycled. This is a strong argument against the up-conversion approach in IR-UWB transmitters since it is highly inefficient to spend several microseconds to start and stop a PLL and then transmit for only a few nanoseconds. (d) Pulse shapes are pre-determined and do not need to change in real time. Even in the case of adaptive pulse shape tuning, the adjustment is needed infrequently, e.g., when the system is powered up or during periodic channel estimations. All these characteristics make a time-interleaved DAC a good candidate for pulse generation of UWB pulses.

\(^1\)Here we intentionally distinguish pulse rate from data rate or symbol rate since each pulse can potentially carry multiple bits of information, and each symbol can have multiple pulses. We also avoid using pulse repetition rate since it may cause confusion in the modulated case.
The technique of time interleaving has been widely used in data converters to achieve higher sampling rate [76]. When multiple DACs are time-interleaved, the overall sampling rate increases to $F_s = f_s \cdot N$, where $f_s$ is the sampling clock frequency controlling each DAC, and $N$ is the number of DACs. For the same sampling rate $F_s$, therefore, the sampling clock frequency $f_s$ is effectively lowered by $N$, and this would significantly reduce the power consumption of each DAC, considering that the power dissipation of CMOS digital circuits is proportional to the clock frequency. This power saving determines that the total power consumption of a time-interleaved structure remains largely constant even when $N$ is large. Therefore, a time-interleaved DAC is well suited for the high sampling rate requirement of IR-UWB pulses. On the other hand, the sampling rate $F_s$ cannot be increased indefinitely by time interleaving. The pole at the output node of high-speed DACs usually dominates the settling time. Apparently, the settling time of each DAC in a time-interleaved architecture needs to be shortened correspondingly to accommodate $N$ samples within each sampling clock cycle $T_s = 1/f_s = N/F_s$, i.e., the sampling period $t_s = 1/F_s = T_s/N$ needs to be greater than the settling time and this eventually limits $F_s$.

Further, the low duty cycle and fixed pulse shapes of IR-UWB pulses mean that the input data rate can be very low. Indeed, the input data can be fixed values, if the number of DACs $N$ is large enough so that the total sampling period $T_s$ of the time-interleaved structure covers the short UWB pulse width. This means the generation and distribution of the input high-speed digital data stream are not needed, and hence can significantly reduce the power consumption of UWB pulse generation. For example, 10-tap time interleaving is sufficient to generate a 1 ns UWB pulse with 100 ps time resolution. The challenge is how to overcome the limitation on the overall sampling rate due to settling time, and how to control the generated pulse shape accurately. In other words, we need to achieve fast settling time while maintaining good amplitude resolution for each DAC. This leads to the development of distributed waveform generator (DWG).
4.3.2 DWG Architecture

A DWG is essentially a special time-interleaved DAC designed for IR-UWB pulse generation, which fully utilizes the properties of IR-UWB pulses. Fig. 4.4 shows the generic architecture of the proposed DWG. In this architecture, a UWB pulse is generated by combining impulses from multiple impulse generators in a time-interleaved fashion. The trigger signal is distributed to each impulse generator by the trigger distribution block, which enables narrow impulses to be generated at specific sampling times. These impulses are then independently conditioned by a pulse conditioner block in each path (called tap), and then combined to form the output pulse waveform by a wideband pulse combining circuit. By changing the characteristics of each impulse generator and conditioner, different output pulse waveforms and spectra can be generated.

There are several distinctive properties of this DWG architecture: First, the trigger signal runs at the pulse rate \( f_P \), which is usually much lower than the Nyquist sampling rate \( F_s \). \( F_s \) is determined by the trigger delay between adjacent taps, and is hence independent of \( f_P \). Generally, low power digital delay lines can be employed for
this trigger distribution. Second, the impulse generators are assisted by the analog pulse conditioner, and isolated from the output. Hence it can be implemented as a digital circuit, optimized for short settling time, and directly benefits from the fast switching characteristics of CMOS transistors. Third, in this architecture, large analog bandwidth is only required for the pulse conditioner and pulse combiner at the output. To address the settling time issue, the DWG utilizes the on-chip transmission lines for the pulse combining. This is similar to the bandwidth challenge in wideband amplifiers, and can be addressed by leveraging distributed circuit techniques [38], as demonstrated below in the prototype DWG implementations. Last, a DWG is fully reconfigurable by tuning the sampling time and pulse width of each impulse generator, as well as the gain of each pulse conditioner.

4.3.3 Peak Sampling

Because UWB pulse spectra are band-pass type (Fig. 4.3), the lack of low-frequency components means that the time domain waveforms show alternating peak points and zero points. The zero points here refer to points with zero (or near zero) amplitudes including zero-crossing points. This is an important characteristic of UWB pulses because it can be utilized to reduce the sampling frequency. Considering two sampling schemes shown in Fig. 4.5, to generate a UWB pulse with 10 GHz bandwidth, the Nyquist sampling requires 20 GHz sampling frequency as in Fig. 4.5 (a). In the other sampling scheme, peak sampling, sampling points are located at the peak points and zero points. Since the samplings at zero points do not need to be generated. The sampling frequency can be effectively reduced by half, 10 GHz in Fig. 4.5 (b). Note that this may introduce some distortion on the signal spectrum since peak points and zeros points may not be uniformly distributed. The pulse spectra generated using Nyquist sampling at 20 GS/s and peak sampling at 10 GS/s are compared in Fig. 4.5 (c), and within 10 GHz bandwidth the distortion is shown to be very small. Therefore peak sampling is an effective scheme to reduce sampling frequency with little distortion.
Figure 4.5: Different sampling schemes to generate UWB pulse: (a) Nyquist sampling; (b) peak sampling; (c) spectra of the sampled signal using these two sampling schemes.
Figure 4.6: Similar to (a) a generic transversal filter, a DWG can be considered (b) a transversal filter with the signal source embedded.

### 4.3.4 Built-in Pulse Shaping

A DWG can also be treated as a transversal finite impulse response (FIR) filter. In a generic transversal FIR filter, input signal $x(t)$ and its delayed versions are multiplied by different coefficients $c_1, c_2, ..., c_N$ and then summed to generate the output signal $y(t)$, as shown in Fig. 4.6. The transfer function of such a FIR filter is determined by the coefficients and the tap delay $\tau$. To see the similarity between the FIR transversal filter and the DWG, the architecture of DWG is re-drawn in Fig. 4.6 (b). Instead of having input signal $x(t)$ fed into the circuit, $x(t)$ is generated locally within each tap by multiple pulse generators. Note that each impulse generator is assumed to generate an identical impulse. The pulse conditioner is used to change the pulse amplitude which is equivalent to multiplying each generated pulse $x(t)$ by a coefficient, so a DWG architecture can realize built-in pulse shaping functions.

The transfer function of a DWG can be described in the time domain as

$$y(t) = \sum_{k=1}^{N} c_k x(t - k\tau)$$  \hspace{1cm} (4.1)

where $c_k$ is the tap coefficient, and $\tau$ is the delay on the trigger distribution. For a
Figure 4.7: IR-UWB pulses and spectra generated using FIR filter (a) $\tau=130$ ps and $N=20$; (b) $\tau=80$ ps and $N=10$. 
typical DWG with uniform $\tau$, the frequency response is given by

$$Y(j\omega) = X(j\omega) \sum_{k=1}^{N} c_k \exp(-j k \omega \tau) = X(j\omega) H(j\omega)$$

(4.2)

where

$$H(j\omega) = \sum_{k=1}^{N} c_k \exp(-j k \omega \tau)$$

(4.3)

Therefore, the output waveform $y(t)$ is determined by three factors, the coefficients, the tap delay and the pulse shape $x(t)$ generated by each pulse generator. $H(j\omega)$ is the same as the FIR filter transfer function. Some example pulses and spectra generated using FIR filter are shown in Fig. 4.7 for low-band and full-band UWB. The tap delay and number of taps are feasible to be implemented using the DWG architecture. The output signal spectrum can be shaped by changing the FIR filter transfer function, or by changing impulse signal spectrum $X(j\omega)$. In practice, due to the minimum achievable pulse width of the impulse signal, $X(j\omega)$ shows a low-pass response which can be used as the reconstruction filter to smooth the output pulse.

The algorithm for pulse synthesis has been developed for the DWG. In the time domain, the output waveform is a weighted sum of delayed narrow pulses generated by each gain cell (Eq. 4.1). Since pulse amplitude can be tuned independently, the impulse generated from each tap are denoted as $b_1(t), b_2(t), \ldots, b_N(t)$. Let the target waveform be described by function $f(t)$, and the delay per tap $\tau$. For the first $\tau$ seconds of $f(t)$, only the pulse response of the first tap is available at the output. So the scaling factor for basis function $b_i(t)$ can be easily determined by correlating the target waveform and the basis function $[59]$}

$$c_i = \frac{\langle b_i(t), f(t) \rangle}{|b_i(t)|^2}$$

(4.4)

### 4.3.5 Modulation Capabilities

Another advantage of the DWG architecture is that pulse modulation, such as on-off keying modulation can be directly achieved by driving the DWG using the
modulated trigger signal. Because the existence and pulse position information of generated UWB pulses can be directly gained from the trigger signal, this one-to-one mapping enables by performing modulation on the trigger signal to achieve equivalent modulation on generated pulses. As shown in Fig. 4.8, the DWG trigger signal can be generated by modulating the periodic clock signal by the baseband data stream. Other modulation schemes, such as pulse position modulation (PPM) can also be applied to the low-speed trigger signal through a digital modulator to move the trigger positions. The positions of output UWB pulses are changed accordingly. Such an implementation does not require analog delay with large signal bandwidth as required if the modulation is performed on generated UWB pulses directly. Thus, low-power digital circuits can be adopted to implement these modulation blocks since the speed requirement is relaxed.
4.3.6 Performance Limitations

Performance limitations for the DWG fall into three categories. First is the speed of each individual pulse generators in the DWG, which is represented by $X(j\omega)$. Narrow pulses are generated in digital pulse generators using the fast switching transistors, but the output part of the pulse conditioner still needs large signal bandwidth. Otherwise, the fast roll-off of $X(j\omega)$ will limit the circuit bandwidth. In the circuit design part of this paper, we will show that the bandwidth of the pulse shaper is the limiting factor for dynamic range in DWG.

Second, the use of time-interleaving introduces the accuracy requirement on timing control. Both systematic timing mismatch and jitter can cause waveform distortion since time delay between neighboring pulse generators directly determines the sampling rate, and they essentially introduce error terms into the FIR response $H(j\omega)$.

Third, the analog bandwidth of the pulse combining block is very important because limited bandwidth can attenuate the pulse amplitude and slow down the rise/fall time of the waveform. To address this issue, a distributed circuit topology based on on-chip transmission lines is utilized in the prototype DWG implementations. Both the pulse combining bandwidth and the timing jitter limit the number of taps for time-interleaving in the DWG architecture, which eventually set an upper limit on the maximum achievable pulse duration.

4.4 Single-Polarity DWG Prototype

4.4.1 Circuit Design

Fig. 4.9 shows a 10-tap DWG prototype implemented in a 0.18$\mu m$ standard digital CMOS technology. It uses an active delay line for trigger distribution, digital pulse generator for basis pulse generation, switched current sources for pulse amplitude control, and an on-chip transmission line for pulse combining.

An asynchronous, current starved active delay line[77] is used for trigger distribution, as shown in (Fig. 4.10 (a)). To achieve 10GS/s sampling rate, the delay per stage
is designed to be nominally 100ps, and can be tuned by varying the delay-tuning voltage $V_{\text{at}}$ in each delay element to change the fall time of the current-starved inverter. In the prototype, a single $V_{\text{at}}$ is used for all delay elements and hence the tap delay is uniform. Non-uniform sampling can be implemented by employing independent delay tuning for each tap. This simplified trigger distribution block can be further improved by using a DLL to achieve better timing control accuracy over the process and temperature variations. Note that a DWG can be directly modulated by using baseband data as trigger.

The impulse generator is designed based on a glitch generator [78], as shown in Fig. 4.10 (b). When a rising-edge comes at the input, a short pulse is generated by the NAND operation of the input step signal and its delayed version. The delay time in the feedback loop, which consists of the propagation delay of NAND gate, the following inverter and the charging time of the NMOS transistor $M_1$, determines the pulse width. Another NMOS transistor $M_3$ is added into the feedback path as a voltage controlled resistor. By varying the width-tuning voltage $V_{\text{wt}}$, the time constant of this charging path changes, which tunes the generated pulse width. Two more inverters serve as the output buffer to drive the following current source.

The generated voltage pulse switches on and off a current source, which is a cascode current mirror. The switched current source is used in the DWG prototype
Figure 4.10: Schematic of the single-polarity DWG prototype: (a) active delay line; (b) impulse generator; (c) switched current source.
Figure 4.11: Chip micrograph of the prototype single-polarity DWG. The meandered output transmission line is connected between two RF pads. The pads at the lower-half chip are for tuning controls and dc bias.

for amplitude tuning, as shown in Fig. 4.10 (c), which is achieved by changing the reference current. When the reference current is tuned to be a very small value, the pole associated with node X becomes the dominant pole since the transconductance of transistor M2 is reduced significantly due to the small current value, as shown in the following equation

\[
\omega_{p,X} = \frac{g_{m2}}{C_X} = \frac{\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}}{2C_{GD1} + C_{DB1} + C_{SB2} + C_{GS2}}
\]  

(4.5)

The bandwidth reduction caused by this dominant pole distorts the impulse shape and eventually limits the dynamic range. The pole associated with mode Y is always at very high frequency because of the small on-resistance of the switching transistor M_{SW}. The outputs of all the current sources are connected to the output transmission line. Such a distributed circuit structure extends the bandwidth at the output node since the parasitic capacitance of all current sources is absorbed into the transmission line structure. The bandwidth of the output node is determined by the capacitively loaded transmission line.

The output transmission line is implemented as a multilayer coplanar waveguide (CPW) transmission line, which builds signal line on top metal layer (M6) and ground
Figure 4.12: Pulses generated by each tap.

plans on a different metal layer (M5). The MCPW has lower loss and larger bandwidth than LC artificial transmission lines [79]. The output impedance is matched to 50 \( \Omega \), which enables the transmitter to drive the antenna directly. Similarly, dual-polarity switched current sources used in the transmitter also have the dynamic range limitation.

Since all building blocks in this DWG implementation are digital/switching circuits except the reference current, it burns little power in stand-by (no trigger), which is highly desirable for low-duty-cycle IR-UWB applications.

The prototype DAWG was fabricated in a commercial 0.18\( \mu m \) standard digital CMOS technology with low-resistivity substrate. The chip micrograph is shown in Fig. 4.11. The chip size is 1.48\( mm \times 1.24mm \), including pads. The active area is 0.68\( mm \times 0.5mm \).

4.4.2 Measurement Results

The prototype DWG is characterized in time domain using a 50 GHz sampling oscilloscope. A 500 MHz sinusoidal signal from a continuous-wave (CW) source is used as the input trigger. The delay uniformity of all ten taps can be observed in Fig. 4.12. They are measured between the middle points of rise edges. The average
Table 4.1: Impulses generated by the single-polarity DWG prototype

<table>
<thead>
<tr>
<th></th>
<th>Min. (ps)</th>
<th>Max. (ps)</th>
<th>Mean (ps)</th>
<th>σ (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tap Delay</td>
<td>73</td>
<td>129</td>
<td>104</td>
<td>15.1</td>
</tr>
<tr>
<td>Rise Time</td>
<td>73</td>
<td>86</td>
<td>79</td>
<td>3.8</td>
</tr>
<tr>
<td>Fall Time</td>
<td>170</td>
<td>183</td>
<td>177</td>
<td>3.2</td>
</tr>
<tr>
<td>Min. Pulse Width</td>
<td>132</td>
<td>143</td>
<td>140</td>
<td>4.6</td>
</tr>
</tbody>
</table>

Figure 4.13: (a) Pulse width tuning (showing only tap1); (b) Delay tuning (showing only tap1 and tap2).

Figure 4.14: (a) Pulse amplitude tuning and (b) corresponding pulse shape change.
tap delay is 104 ps with a standard deviation \( \sigma \) of 15.1 ps, which corresponds to a sample rate of 10 GS/s. The last delay element does not have a load, which causes a delay (73 ps) much smaller than others. On average, the rise time is 79 ps with a \( \sigma \) of 3.8 ps, the fall time is 177 ps with a \( \sigma \) of 3.2 ps, and the minimum pulse width is 140 ps with a \( \sigma \) of 4.6 ps. The pulse width of all taps can be tuned from 140 ps to over 1 ns (Fig. 4.13 (a)). The average tap delay can be tuned over a range of 104 ps to 144 ps, which provides the capability of changing sampling rate. Characterization results are summarized in Table 4.1.

By varying the reference current of the switched current mirrors, the individual output pulse amplitudes can be independently tuned. The pulse amplitude tuning has good linearity within a 10 dB dynamic range (Fig. 4.14 (a)). The pulse shape is also well conserved when tuning the pulse amplitude, and is quantified with the correlation factor defined in Eqn. 4.6 below.

\[
Corr = \frac{\int_{-\infty}^{+\infty} f_1(t) \cdot f_2(t) dt}{\sqrt{\int_{-\infty}^{+\infty} f_1^2(t) dt \cdot \int_{-\infty}^{+\infty} f_2^2(t) dt}}
\]  

(4.6)

Within the dynamic range of about 10 dB, the correlation factor is more than 0.9, as shown in Fig. 4.14 (b). In these measurements, the DWG is biased to achieve minimum delay and minimum pulse width.

Since time-interleaved circuits are sensitive to timing error, jitter performance is characterized at the transmitter output for each generated impulse. Due to the small duty cycle of the impulse, self-reference jitter measurement is not feasible. So the input trigger signal is split to trigger the oscilloscope. The RMS jitter is 2.2 ps and the peak-to-peak jitter is 13.8 ps. The input trigger signal has a measured RMS jitter of 1.6 ps. So the additive RMS jitter from the prototype DWG is only about 1.5 ps. These values are much smaller than normal 100 ps tap delay, so the pulse shape distortion caused by the jitter is negligible.

Fig. 4.15 shows synthesized sinusoidal waveforms and UWB waveforms with their corresponding spectra. The first sinusoidal waveform has a fundamental frequency of 930 MHz, and the SFDR is 30 dBc. The second sinusoidal has a peak frequency
Figure 4.15: Example waveforms synthesized using the prototype DWG.

Figure 4.16: Output waveform of the prototype DWG driven by PRBS data.
Table 4.2: Performance summary of the single-polarity DWG prototype

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.18µm Digital CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply</td>
<td>1.8V</td>
</tr>
<tr>
<td>Maximum PRF</td>
<td>1.1GHz</td>
</tr>
<tr>
<td>Tunable time resolution</td>
<td>104ps-150ps</td>
</tr>
<tr>
<td>Tunable pulse width</td>
<td>140ps-1ns</td>
</tr>
<tr>
<td>Pulse amplitude</td>
<td>110mV</td>
</tr>
<tr>
<td>Amplitude tuning dynamic range</td>
<td>10dB</td>
</tr>
<tr>
<td>Maximum power consumption</td>
<td>50mW for 1GHz PRF</td>
</tr>
<tr>
<td>Power efficiency</td>
<td>50pJ/b</td>
</tr>
</tbody>
</table>

Table 4.3: Comparison of the single-polarity DWG prototype with other reported work

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Technology</th>
<th>Power (mW)</th>
<th>Data rate (Mbps)</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>[68]</td>
<td>0.18µm CMOS</td>
<td>76</td>
<td>400</td>
<td>190</td>
</tr>
<tr>
<td>[80]</td>
<td>0.25µm SiGe BiCMOS</td>
<td>66</td>
<td>500</td>
<td>132</td>
</tr>
<tr>
<td>[69]</td>
<td>0.13µm CMOS</td>
<td>10</td>
<td>160</td>
<td>62.5</td>
</tr>
<tr>
<td>This work</td>
<td>0.18µm CMOS</td>
<td>50</td>
<td>1000</td>
<td>50</td>
</tr>
</tbody>
</table>

\[ FOM = \frac{\text{Power}}{\text{Data rate}} \]
at 4.5 GHz, close to the Nyquist rate. The UWB pulses include monocycle, doublet and 5th Gaussian derivative, with the center frequency from 2 to 4 GHz. Note that we use a sinusoidal (CW) signal source as the trigger in these tests. Pulse repetition rate up to 1.1 GHz can be sustained, which shows that a DWG can be used for high data-rate applications. Since the prototype is designed with single-polarity pulses, these pulses are generated with dc offset on-chip (ac coupled off-chip), which causes some asymmetry in the waveform and also the spectrum distortion.

Fig. 4.16 shows the on-off keying modulation of the prototype driven by a 32-bit, 16Mbps pseudo random bit stream (PRBS) with a Gaussian basis pulse. The small fluctuation on the waveform amplitude is caused by the limited number of sampling points (4096pts) in the measurement window. A DWG’s power consumption is proportional to the pulse repetition frequency (PRF), which is about 25mW at 500MHz and 50mW at 1GHz. The prototype performance is summarized and compared with other reported work in Table 4.2 and Table 4.3.

4.5 Dual-Polarity DWG Prototype for IR-UWB Transmitter

4.5.1 Circuit Design

Fig. 4.17 shows the architecture of proposed DWG-based IR-UWB transmitter. The transmitter integrates a modulator for pulse position modulation (PPM) and a DWG. The input trigger signal from baseband processor is modulated by the PPM
Figure 4.18: Overall schematic of the dula-polarity DWG based IR-UWB transmitter.

signal first, and then distributed to the DWG to generate the target UWB waveforms. In such a transmitter architecture, the modulation is performed the trigger signal instead of generated short pulses to reduce the circuit speed requirement. Hence, low-power digital circuits can be employed to implement both PPM modulator and trigger distribution block.

Fig. 4.18 shows the detailed schematic of the IR-UWB transmitter. The modulation and time interleaving are performed on the relatively low-speed trigger signal. It uses a digital modulator for pulse position modulation, an active delay line for trigger distribution, digital impulse generator for dual-polarity basis pulse generation, dual-polarity switched current sources for pulse amplitude control, and an on-chip transmission line for pulse combining.

An asynchronous, current starved active delay line [77] is used for trigger distribution. To achieve 10GS/s sampling rate, the delay per stage is designed to be nominally 100ps, and can be tuned by varying the delay-tuning voltage $V_{dt}$ in each delay element to change the fall time of the current-starved inverter. A delay-locked loop (DLL) configuration can be used to improve the timing accuracy over PVT variations.
Figure 4.19: Schematic of the dual-polarity DWG based IR-UWB transmitter: (a) impulse generator; (b) dual-polarity switched current source; (c) pulse position modulator.
Different from the single-polarity DWG [75], the impulse generator is designed to generate both positive and negative impulses, as shown in Fig. 4.19 (a). When a rising edge arrives at the trigger input, if the polarity control signal is high, it is steered to the upper signal path and a short negative impulse is generated by the NAND operation of the input step signal and its delayed version. On the other hand, if the polarity signal is low, the input trigger is steered to the lower signal path and a short positive impulse is generated by the NOR operation of the input step signal and its delayed version. This topology can obtain both positive and negative impulses which are needed to control the dual-polarity switched current source.

Due to the use of static CMOS logic for trigger distribution and impulse generators, achievable minimum tap delay and pulse width are determined by the propagation delay of full swing signals along CMOS gates. Smaller delay and faster rise time can be achieved by using the current mode logic (CML) at the cost of static power consumption and extra CML-CMOS conversion circuits.

The generated short voltage pulse switches on and off the dual-polarity switched current source (Fig. 4.19 (b)), which injects the short current pulses into the output transmission line. The amplitude of the output current pulse can be independently controlled by varying the reference current of the current mirror. The outputs of all the current sources are connected to the output transmission line. Such a distributed
Figure 4.21: Impulses generated by all DWG taps in the prototype transmitter, showing only the negative pulses.

circuit structure extends the bandwidth at the output node since the parasitic capacitance of all current sources is absorbed into the transmission line structure. The output transmission line is implemented as a coplanar waveguide (CPW) transmission line, which has lower loss and larger bandwidth than LC artificial transmission lines [79]. The output impedance is matched to 50Ω, which enables the transmitter to drive the antenna directly. Dual-polarity switched current sources used in the transmitter also have the dynamic range limitation as in the single-polarity DWG.

The schematic of digital pulse position modulator is shown in Fig. 4.19 (e). Knowing basis pulses are generated at the rising edge of each trigger signal, the pulse position modulation is obtained by simply splitting the trigger signal into two and delaying one of them by a time delay Δ-PPM. After that, a 2:1 multiplexer controlled by the PPM data selects one of these two delayed trigger signals to determine the pulse position.

The prototype transmitter was fabricated in a commercial 0.18μm standard digital CMOS technology with low-resistivity substrate. The chip micrograph is shown in Fig. 4.20. The circuit area is 1.6mm × 0.2mm. The chip size including pad frame is 2.8mm × 1.8mm.
Table 4.4: Impulse generated by the dual-polarity DWG prototype

<table>
<thead>
<tr>
<th></th>
<th>Min. (ps)</th>
<th>Max. (ps)</th>
<th>Mean (ps)</th>
<th>σ (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tap Delay</td>
<td>90</td>
<td>98</td>
<td>94</td>
<td>3.1</td>
</tr>
<tr>
<td>Rise Time</td>
<td>66</td>
<td>75</td>
<td>70</td>
<td>3.2</td>
</tr>
<tr>
<td>Fall Time</td>
<td>106</td>
<td>117</td>
<td>112</td>
<td>3.5</td>
</tr>
<tr>
<td>Min. Pulse Width</td>
<td>112</td>
<td>125</td>
<td>120</td>
<td>4.6</td>
</tr>
</tbody>
</table>

Figure 4.22: (a) impulse width tuning and (b) tuning tap delay, showing only impulses from tap1 and tap2.
4.5.2 Measurement Results

The transmitter is characterized in time domain using a 50 GHz sampling oscilloscope. First, the DWG core is tested with a 200 MHz sinusoidal signal from a continuous-wave (CW) signal source as the input trigger without any modulation. Fig. 4.21 shows the impulse waveforms generated from all taps at the output, when the delay between neighboring taps is tuned to minimum. Measured between the middle points of rise edges, the average tap delay is 94 ps with a standard deviation $\sigma$ of 3.1 ps, which corresponds to a sample rate of 10.6 GS/s. The tap delay uniformity is evident. The rise time of each impulse is 70 ps in average with a $\sigma$ of 3.2 ps, the fall time is 112 ps with a $\sigma$ of 3.5 ps, and the minimum pulse width is 120 ps with a $\sigma$ of 4.6 ps. Further, the tap delay can be tuned up to 190 ps (Fig. 4.22), and the impulse width of all taps can also be tuned from 120 ps to 0.7 ns as summarized in Table 4.4.

The long-term RMS jitter of each impulse is found to be 2.4 ps. and the peak-to-peak jitter is 14.2 ps. The input trigger signal has a measured RMS jitter of 1.6 ps. Both include the jitter from the oscilloscope trigger circuitry. Hence the jitter generation in the prototype transmitter is only about 1.7 ps, which should be negligible for IR-UWB applications.

Fig. 4.23 shows generated UWB waveforms with their frequency spectra. The first UWB waveform shown in Fig. 4.23 (a)(b) is a doublet with a duration of 0.5 ns, generated by tap 1, 2 and 3. The corresponding spectrum has a center frequency of 3 GHz and a -10 dB bandwidth of 5 GHz. Better frequency resolution can be achieved using more taps. One example is shown in Fig. 4.23 (c)(d). The complex waveform in time domain has a duration of 0.8 ns and 40 mV maximum amplitude, generated by 8 taps. It shows a well matched frequency spectrum with the FCC mask. The -10 dB bandwidth of the signal spectrum covers 3 GHz to 8 GHz, with the peak at about 6 GHz. At 10 GHz, the power spectrum density only drops by about -14 dB. The large signal bandwidth can provide more signal power and processing gain, so the spectrum efficiency is improved. These generated waveforms with different spectra demonstrate the reconfigurability of DWG based transmitter.

OOK and PPM modulations are also tested for the prototype transmitter. Fig. 4.24
Figure 4.23: Some measured UWB waveforms and their spectra from the dual-polarity DWG based transmitter.
Figure 4.24: OOK modulation using 32 Mbps PRBS data.
Figure 4.25: Measured output waveforms at 2.5 GHz, 1.5 GHz and 500 MHz pulse rate.
Figure 4.26: Tunable $\Delta$-PPM from 200 ps to 400 ps.

shows the on-off keying modulation of the transmitter driven by a 32-bit, 32Mbps pseudo random bit stream (PRBS) with a UWB output waveform. The UWB pulse train is generated corresponding to the input data stream. The fluctuation on the waveform amplitude is caused by the limited number of sampling points (4096pts) in the measurement window. To demonstrate the transmission at variable data rate up to Gbps, the transmitter prototype is tested at pulse rate higher than the nominal design value (2.5 GHz, 1.5 GHz and 500 MHz). Generated UWB pulse waveforms are shown in Fig. 4.25. In the 2.5 GHz case, since the period is only 400 ps, generated pulses are little distorted compared to lower pulse rate cases.

Fig. 4.26 shows the time domain characterization of binary PPM. The $\Delta$-PPM is tunable from 200 ps to 400 ps. Time waveforms of PPM are show in Fig. 4.27. In this test, the DWG is driven by 200 MHz clock signal and modulated by 40 MHz square wave. Output UWB sequences without and with PPM modulation are both shown to demonstrate position shift when the modulation signal is applied. The power consumption of the transmitter is proportional to the pulse rate. In the OOK, since there is little power transmitted for bit 0, the power consumption is only 25pJ/b. In the PPM, the power consumption is about 45pJ/b. Table 4.5 summarizes the performance of the proposed IR-UWB transmitter, which demonstrate important
Figure 4.27: Measured PPM output waveforms modulated at 40 MHz, driven at 200 MHz.
Table 4.5: Performance summary of the DWG based IR-UWB transmitter

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.18μm Digital CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply</td>
<td>1.8V</td>
</tr>
<tr>
<td>Transmitted Power</td>
<td>-7dBm</td>
</tr>
<tr>
<td>Pulse Width</td>
<td>0.8ns</td>
</tr>
<tr>
<td>Pulse Bandwidth</td>
<td>6GHz (3-9GHz)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>45pJ/pulse</td>
</tr>
<tr>
<td>Data Rate</td>
<td>10kbps-1Gbps (variable)</td>
</tr>
<tr>
<td>Modulation</td>
<td>OOK, PPM</td>
</tr>
</tbody>
</table>

Table 4.6: Performance comparison with other reported high-speed DACs

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Power (mW)</th>
<th>Bits</th>
<th>$F_s$ (GS/s)</th>
<th>FOM1 (pJ/S)</th>
<th>FOM2 (pJ/S)</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>[81]</td>
<td>12</td>
<td>5</td>
<td>10</td>
<td>0.0375</td>
<td>0.24</td>
<td>0.18μm SiGe</td>
</tr>
<tr>
<td>[71]</td>
<td>360</td>
<td>6</td>
<td>20</td>
<td>0.28</td>
<td>3</td>
<td>0.18μm SiGe</td>
</tr>
<tr>
<td>[82]</td>
<td>29</td>
<td>6</td>
<td>3</td>
<td>0.151</td>
<td>1.61</td>
<td>0.13μm CMOS</td>
</tr>
<tr>
<td>[83]</td>
<td>190</td>
<td>8</td>
<td>12</td>
<td>0.0618</td>
<td>1.98</td>
<td>0.09μm CMOS</td>
</tr>
<tr>
<td>[84]</td>
<td>1014</td>
<td>6</td>
<td>22</td>
<td>0.72</td>
<td>7.68</td>
<td>0.13μm SiGe</td>
</tr>
<tr>
<td>[85]</td>
<td>455</td>
<td>4</td>
<td>30</td>
<td>0.92</td>
<td>3.75</td>
<td>0.25μm SiGe</td>
</tr>
<tr>
<td>[86]</td>
<td>150</td>
<td>4</td>
<td>10</td>
<td>0.94</td>
<td>3.75</td>
<td>0.13μm CMOS</td>
</tr>
<tr>
<td>[87]</td>
<td>660</td>
<td>3</td>
<td>40</td>
<td>2.75</td>
<td>5.5</td>
<td>0.12μm SiGe</td>
</tr>
<tr>
<td>This work</td>
<td>50</td>
<td>3</td>
<td>10</td>
<td>0.625</td>
<td>1.66</td>
<td>0.18μm CMOS</td>
</tr>
</tbody>
</table>

\[
FOM1 = \frac{P}{2^{N_f_s}}; \quad FOM2 = \frac{P}{N_f_s}
\]

features including low power consumption, large signal bandwidth, variable data rate and modulation capabilities. The comparison of DWG with other reported GS/s DACs implemented in advanced technologies is listed in Table 4.6. Implemented in the low cost CMOS technology, the DWG achieves comparable performance in terms of sampling frequency, dynamic range while consuming less power.
4.6 DAC-Assisted DWG with Current-Steering Pulse Generators

4.6.1 Circuit Design

Fig. 4.28 shows a 64-tap DWG prototype implemented in a 0.18μm standard digital CMOS technology. It uses an active delay line for trigger distribution, DAC assisted pulse generators for basis pulse generation with pulse amplitude control, and an on-chip transmission line for pulse combining. 64 pulse generators are arranged in a 8 by 8 matrix over the entire chip. A 6-bit decoder is also included to select which pulse generator to write the amplitude data. An asynchronous, current starved active delay line[77] is used for trigger distribution. To achieve 10GS/s sampling rate, the delay per stage is designed to be nominally 100 ps.

The DAC assisted pulse generator is shown in Fig. 4.29 (a). It consists of a 7-bit register and a pulse generator array. The register is used to store the amplitude data and enable the corresponding number of unit pulse generators inside the array. The pulse generator array has 127 unit pulse generators with 7-bit digital control, as in
Figure 4.29: Schematic of the prototype DWG: (a) DAC assisted pulse generator; (b) pulse generator array; (c) new current-steering pulse generator.
Fig. 4.29 (a). The topology of each unit pulse generator is shown in Fig. 4.29 (b). Compared to the conventional current steering structure, this new topology incorporates the edge combiner, which is formed by $M_1$ and $M_2$. At the initial state, it is assumed that all the current flows through $M_1$. When the pulse generator is triggered by a rising edge, the falling edge on $M_1$ gate will turn it off so that all the current is steered through $M_3$. A delayed rising edge will turn on $M_2$ afterwards and the current is steered through $M_2$. Hence, a very short current pulse is generated at the output of $M_3$. At the falling edge of the input trigger, the current will be steered from $M_2$ back to $M_1$, which does not affect the status of $M_3$. So this pulse generator is rising edge sensitive only. The timing diagram of the current-steering pulse generator is also shown in Fig. 4.29 (b).

The outputs of all the pulse generators are connected to the output transmission line. Such a distributed circuit structure extends the bandwidth at the output node since the parasitic capacitance of all pulse generators is absorbed into the transmission line structure. The output transmission line is implemented as a coplanar waveguide (CPW), which has lower loss and larger bandwidth than LC artificial transmission lines.

The 64-tap DWG prototype was also fabricated in 0.18 $\mu$m standard digital CMOS technology with low-resistivity substrate. The chip micrograph is shown in Fig. 4.30.
The chip size is $2.9mm \times 3.1mm$, including pads.

### 4.6.2 Measurement Results

The prototype DWG is characterized in time domain using a 50 GHz sampling oscilloscope. A 200 MHz sinusoidal signal from a continuous-wave (CW) source is used as the input trigger. The measured basis pulses generated from all 64 taps are in Fig. 4.31 which shows good delay uniformity. As shown in Fig. 4.32 (a), the average tap delay is 91.8 ps with a standard deviation $\sigma$ of 1.9 ps, which corresponds to a sample rate of 10.9 GHz. As shown in Fig. 4.32 (b), on average, the rise time
Figure 4.33: Using Tap1 as example (a) Pulse amplitude tuning and (b) corresponding pulse shape change.

\[
\text{Corr} = \frac{\int f_1(t) \cdot f_2(t) dt}{\sqrt{\int f_1^2(t) dt} \cdot \sqrt{\int f_2^2(t) dt}}
\]
is 70.3 ps and for the first 20 taps, the rise time is always less than 60 ps. The amplitude of basis pulses decreases in an exponential fashion because of the loss on the on-chip transmission line. The loss factor of the transmission line is extracted to be 0.85dB/mm. The rise time increases because of the bandwidth reduction caused by the transmission line loss.

By varying the digital control words, the output pulse amplitude can be independently tuned. Fig. 4.33 shows the amplitude tuning of taps as an example. The pulse amplitude tuning has good linearity within a 20 dB dynamic range. The pulse shape is also well conserved when tuning the pulse amplitude, and is quantified with the correlation factor (Fig. 4.33 (b)), where the maximum amplitude pulse is selected as the reference. For all the control words, the correlation factor is more than 0.96, which means the pulse shape is well conserved when the amplitude is tuned.

Jitter performance of some taps is shown in Fig. 4.34. The average RMS jitter is 11 ps. The RMS jitter remains less than 10 ps until Tap30 and increases about 20 ps for the last few taps. The jitter is expected to increase monotonically along the active delay line as the number of taps increases. However, in the measurement, we observe the minimum jitter point at around tap 18. This is because 200 MHz sinusoidal signal is used to trigger the DWG, in which the slope is not sharp enough so that both the amplitude noise and the phase noise can contribute to the jitter. After passing several inverters in the active delay line, the edge becomes sharper and
Figure 4.35: Some example waveforms generated using the DWG prototype. (a) using tap1,2,3; (b) using tap1 to tap10.
Figure 4.36: Proposed IR-UWB transmitter with M-ary pulse shape modulation.

sharper which suppress the effect of amplitude noise on the jitter performance. This is why the minimum jitter point occurs at around tap 18. After that, noise from the power supply and other sources adds to the phase noise gradually, which cause the increase of jitter. Some square waveforms with different duration (200 ps and 800 ps) are generated using the DWG prototype, as in Fig. 4.35.

4.7 DWG Based IR-UWB Transmitter with Pulse Shape Modulation

4.7.1 Circuit Design

The reconfigurability of DWG can be utilized to implement the pulse shape modulation (PSM) scheme in IR-UWB transmitter. The M-ary PSM transmitter architecture is shown in Fig. 4.36. It incorporates M DWGs to generate M orthogonal pulse shapes. To which DWG the trigger signal is distributed is determined by the input data stream using the DEMUX. The same pulse combining block is used for all DWGs.

As a demonstration, IR-UWB transmitter prototype with binary pulse shape modulation is implemented in digital CMOS technology. The transmitter schematic is shown in Fig. 4.37, which uses two DWGs with two active delay line for trigger distribution, and one on-chip transmission line for pulse combining. To improve the match,
pulse generators of two 20-tap DWGs are interdigitized along the output transmission line. By this arrangement, the mismatch from active delay line jitter and transmission line loss can be greatly reduced. Each pulse generator is a 7-bit DAC-assisted dual-polarity pulse generator.

The design of the DAC-assisted dual-polarity pulse generator is shown in Fig. 4.38 (a), which includes the switched current source array and the 7-bit register. The switched current source array has 64 switched current source units. The schematic of the switched current source unit is shown in Fig. 4.38 (b). The impulse generator design is the same as in Fig. 4.19 (c). Generated voltage switching signals from the impulse generator are input to $SW_n$ or $SW_p$ to switch on and off the transistors. $EN_n$ and $EN_p$ signals are determined by the input amplitude data to enable each switched current source unit. Since switching transistors are isolated from the output node by two transistor, the clock feedthrough effect is greatly mitigated.

The outputs of all 40 DAC-assisted dual-polarity pulse generators from two DWGs are connected to the output transmission line in a interdigitized fashion. Such a distributed circuit structure extends the bandwidth at the output node since the parasitic capacitance of all current sources is absorbed into the transmission line

Figure 4.37: Schematic of the DWG based IR-UWB transmitter with binary pulse shape modulation.
Figure 4.38: (a) Schematic of the DAC-assisted pulse generator; (b) dual-polarity switched current source.
Figure 4.39: Chip micrograph of the prototype IR-UWB transmitter with pulse shape modulation.

Figure 4.40: Pulses generated by each tap in one 20-tap DWG.

structure.

The prototype transmitter was fabricated in a commercial $0.18\mu m$ standard digital CMOS technology with low-resistivity substrate. The chip micrograph is shown in Fig. 4.39. The chip size including pad frame is $3.2\,mm \times 2.2\,mm$.

4.7.2 Measurement Results

This IR-UWB transmitter prototype includes two 20-tap DWG inside. One 20-tap DWG is characterized in time domain using a 50 GHz sampling oscilloscope. A 200 MHz sinusoidal signal from a continuous-wave (CW) source is used as the input
Figure 4.41: (a) Generated pulses with BPSK modulation; (b) Generated pulses with PSM.
Figure 4.42: (a) Generated orthogonal pulses for PSM; (b) (c) Measured spectra of the two orthogonal pulses.
trigger. The measured basis pulses generated from all 20 taps are in Fig. 4.31 which shows good delay uniformity. The average tap delay is about 167 ps, larger than the expected 100 ps.

In the measurement, two modulation schemes are demonstrated. In Fig. 4.41 (a), binary phase shift keying (BPSK) is shown using simple Gaussian monocycle pulses. In Fig. 4.41 (b), pulse shape modulation is shown using Gaussian monocycle pulses and doublet pulses.

By using more taps in the two DWGs, orthogonal pulses based on prolate spheroidal wave functions (PSWF) have been generated, as shown in Fig. 4.42 (a). They have the same 2 ns pulse duration. The correlation factor between these two pulses is only 0.1, which can verify the orthogonality. The measured spectra of these two pulses are shown in Fig. 4.42 (b) (c), which shows that the main lobes of the spectra are almost identical. This is expected according to the characteristics of PSWF. By using this set of orthogonal pulses, the bandwidth required for pulse transmission is maintained, which is critical to satisfy the FCC mask.

4.8 Summary

We have developed a distributed waveform generator (DWG) architecture. A 10-tap, 10GS/s prototype was designed and implemented in a 0.18\(\mu m\) standard digital CMOS technology. Measurement results demonstrated its capability of synthesizing various pulse shapes in sub-nanosecond regime. Testing results of On-off keying modulation using 16 Mbps PRBS data are also presented. The DWG consumes maximal 30 mW at 500 MHz pulse repetition rate, and 50 mW at 1 GHz.

A new impulse radio UWB transmitter is demonstrated with a chip prototype implemented in a 0.18\(\mu m\) standard digital CMOS technology. Its core is a 10-tap, 10GS/s distributed waveform generator (DWG), a newly-developed time-interleaved pulse circuit. Measurement results demonstrated its capability of synthesizing arbitrary pulse waveforms with sub-nanosecond time resolution and compliant the FCC emission mask. Digital modulation schemes such as OOK and binary PPM are readily integrated in the DWG-based transmitter, and demonstrated using 32 Mbps PRBS
data. The transmitter consumes 25pJ/b in OOK and 45pJ/b in PPM.

A distributed waveform generator (DWG) architecture with DAC assisted pulse generator has been developed to achieve longer pulse duration and improve the dynamic range of amplitude tuning. A new high-speed current-steering pulse generator topology is developed by incorporating the edge combiner to generate narrow pulses. A 64-tap prototype was designed and implemented in a 0.18\(\mu\)m standard digital CMOS technology. Measurement results demonstrated its capability of synthesizing various pulse shapes in sub-nanosecond regime for laser system applications.

DWG based IR-UWB transmitter with pulse shape modulation is also demonstrated. Two generated pulses based on PSWF have similar spectrum and pulse duration, with a correlation factor of 0.1.
Chapter 5

Distributed Pulsed Correlators

This chapter presents a new high-speed pulse circuit technique, *distributed pulsed correlator* (DPC), for IR-UWB applications. A DPC time-interleaves multiple analog pulsed multipliers. Each multiplier is triggered by an impulse generated locally to sample the input UWB pulse at a specific time, and then multiplies the sample within the impulse duration by a tunable coefficient. All multiplier outputs are integrated together to generate the correlation output. Since the local template pulse generator is built into the DPC as the sequence of sampling impulses and analog multiplication coefficients, the receiver architecture based on DPC can be greatly simplified. A DPC is low power and fully reconfigurable compared to other UWB pulse detection approaches based on analog correlation. A 8-tap, 10GSample/s DPC prototype was designed and implemented in 0.18\( \mu \)m standard digital CMOS. The prototype achieves an energy efficiency of 40pJ/pulse for 250MHz pulse rate in the measurement.

5.1 Introduction

IR-UWB has great potential in low data-rate wireless communications such as sensor networks because of its promised low circuit complexity, low power consumption, and location capability [23]. Although low-power solutions have been demonstrated for transmitters [88, 75], the design for low-power IR-UWB receiver remains challenging. Analog front-end requires very large bandwidth (5-10GHz) to maintain the pulse
shape. Accurate timing and signal synchronization in the 100 ps range are necessary to detect the pulse position. Baseband processing also needs high sampling rate data converters. All these are still impediments in the implementations of a low-power IR-UWB receiver.

![IR-UWB receiver architecture](image)

Figure 5.1: IR-UWB receiver architecture based on conventional analog correlation.

Several different receiver topologies have been proposed for IR-UWB communication, including the direct conversion [89, 90], analog correlation [68, 91], and transmitted reference [92]. In a direct conversion IR-UWB receiver, the received pulses are, after a down-conversion to baseband, directly sampled by high-speed ADCs and further processed in the digital domain. This provides the implementation of correlation and filtering in digital domain. But the high-speed ADC consumes significant amount of power which is not acceptable to battery powered mobile devices. In order to avoid the use of high-speed ADCs, an analog correlation receiver (Fig. 5.1) moves the matched filter function from digital domain to the analog front-end by correlating the received UWB pulses with a locally-generated template pulse. This topology can reduce the required sampling frequency of ADCs from Nyquist rate to pulse rate, which greatly reduce their power consumption.

Based on these design considerations, the analog correlation topology (Fig. 5.1) is more suitable for the implementation of low-power IR-UWB receivers. There are two challenges in this architecture: correlation and local template pulse generation. The latter one needs to be both low-power and reconfigurable for different channel environments. To circumvent the problem, a transmitted reference transceiver transmits a reference pulse along a data pulse, and the reference pulse is correlated with the
data pulse in the receiver. This topology, however, suffers large performance degrada-
tion due to the noisy received template, and faces a new difficulty in wideband
analog delay line.

![Figure 5.2: IR-UWB transceiver architecture based on DWG and DPC.](image)

A conventional correlator consists of a multiplier and an integrator (Fig. 5.1), and
the correlation function is achieved by multiplying the incoming UWB pulses with
local template pulses and integrating over the pulse duration time. Multiplier-based
correlators have been proposed for most IR-UWB transceivers. In [93], a broadband
CMOS multiplier-based correlator is proposed for a full-band IR-UWB receiver, but
the power consumption (52mW) is fairly large for low data-rate applications. In [94],
dynamic bias control is introduced to reduce the power consumption of an analog
correlator by duty-cycle the multiplier, i.e., it only operates when the local template
pulse is on. But the local template pulse generator is still needed to realize the
correlation function. In this chapter, a distributed pulsed correlator (DPC) with built-
in local template pulse generator is proposed to achieve low power consumption and
simplified architecture for IR-UWB receivers. The IR-UWB transceiver architecture
based on DWG and DPC are shown in Fig. 5.2, which does not have the local template
pulse generator.
5.2 Distributed Pulsed Correlator Architecture

Recently, distributed architecture has been applied into the waveform generation circuit, i.e. distributed waveform generator (DWG), as the core circuit of an IR-UWB transmitter [75]. DWG-based IR-UWB transmitter enables generating low data-rate signals with high sampling rate and low power consumption simultaneously. To leverage the benefits of distributed architectures in UWB pulse processing, here we propose a new analog correlator for IR-UWB pulse detection. The generic architecture of such a distributed pulsed correlator (DPC) is shown in Fig.5.3. A DPC time-interleaves multiple pulsed multipliers in parallel. Received pulses are distributed to these pulsed multipliers by the power distribution block, and correlated by multiple pulsed multipliers in sequence. Each pulsed multiplier is triggered by an impulse $P_i$ generated by the impulse generator at a specific time, and multiplies the UWB pulse within the impulse duration by a tunable gain $g_i$. This is equivalent to correlating the UWB pulse with a sequence of narrow impulses with tunable amplitude, as illustrated by the $P_i \cdot g_i$ impulses in Fig. 5.3. The combination of these impulses essentially forms the local template pulse. All multiplier outputs are integrated to give the overall correlation output. Different from the conventional correlator, the template generator is essentially built in a DPC and distributed over these pulsed multipliers.

Such a distributed correlator architecture allows the detection of UWB pulses with
Figure 5.4: Overall schematic of the differential DPC prototype.

very high sampling rate while maintaining a low data-rate. The high sampling rate is ensured by the small delay between neighboring taps in the trigger distribution. Because UWB pulses are band-pass signals, the peaking sampling scheme used in the DWG design also applies in the DPC design. By using a sequence of narrow impulses to sample the UWB pulse at peak points, the sampling frequency is reduced by half, which means 100 ps time resolution would be enough to provide 20 GHz sampling frequency with little distortion. But it requires very accurate timing control on the sampling points. Since pulsed multipliers only consume switching power, this is especially efficient for low duty-cycle signal detection. The transversal structure also implies the capability of correlating with reconfigurable local templates. The output signals of all the pulsed multipliers are integrated to generate the correlation output so the power loss on the drain termination in a conventional distributed front-ends [95] is saved.

5.3 Differential DPC Prototype

5.3.1 Circuit Design

Fig. 5.4 shows the schematic of a prototype 8-tap distributed pulsed correlator. The trigger signal is distributed through an asynchronous, current starved active
Figure 5.5: Schematic of the pulsed multiplier with built-in impulse generator.

Figure 5.6: Simulation results of the DPC prototype.
delay line. The delay per stage is designed at nominally 100 ps, which corresponds to a sampling rate of 10 GS/s. Received UWB pulse is distributed to each pulsed multiplier by a differential on-chip transmission line, which is implemented using the multi-layer coplanar waveguide (MCPW) [79], and exhibits lower loss and larger bandwidth than LC artificial transmission lines. Output currents from each pulsed multiplier are integrated on capacitors $C_1$ and $C_2$. After the correlation operation and the hold time, switch $S_1$ and $S_2$ reset the voltage level on $C_1$ and $C_2$. DC offset and $1/f$ noise effects on the integration capacitors are greatly reduced since for most time between two pulse detections, integration capacitors are reset to have a constant voltage.

The schematic of the pulsed multiplier is shown in Fig. 5.5. The pulsed multiplier has two functions: sampling the UWB pulse and multiplying the sampled signal by a tunable coefficient. The trigger signal is switched between two paths according to the polarity of the UWB pulse to be detected. Within either signal path of the impulse edge generation, the trigger signal is further split to generate a rising edge and a delayed falling edge. These two edges switch on and off two source transistors $M_5$ $M_6$ or $M_7$ $M_8$, to generate a narrow current impulse. This current impulse sets the transconductance of the differential pair $M_1$ $M_2$ or $M_3$ $M_4$. The amplitude of current impulse can be tuned by changing the reference bias current. Within this
short duration of current impulse, differential pair $M_1 M_2$ or $M_3 M_4$ multiplies part of the input UWB pulse with the transconductance. So the local template pulse shape is determined by the various transconductance of each pulsed multiplier.

This pulsed multiplier topology also benefits the integrator design. When $M_5 - M_8$ are switched off, the output impedance of each pulsed multiplier is very high, so the leakage problem on the integration capacitor is greatly mitigated compared to the conventional multiplier-based correlators. Thus small size of integration capacitor can be used to improve the conversion gain.

Simulation results of the DPC prototype with differential UWB pulse input are shown in Fig. 5.6. Short current pulses generated inside three pulsed multipliers are aligned with major peaks of the input UWB pulses to perform correlation. Two correlator output waveforms have a DC level of 1.3 V, with small fluctuation caused by the correlation operation. The differential correlator output shows clearly that there are three jumps at the rising edge at the correlation phase. Since all building blocks implemented in this pulsed correlator are digital/switching circuits except the reference current, it burns little power in stand-by (no trigger), which is highly desirable for low-duty-cycle IR-UWB applications.

The prototype correlator was fabricated in a commercial 0.18$\mu$m standard digital CMOS technology with low-resistivity substrate. The chip micrograph is shown in Fig. 5.7. The chip size including pad frame is $1.8mm \times 1.5mm$. The active area is shown in the dash box, which is only about $0.36mm^2$.

### 5.3.2 Measurement Results

The DPC test is performed in time domain, and the test setup is shown in Fig. 5.8. Input Gaussian-shape pulse $V_s$ is generated by the impulse generator, which is modulated by baseband data stream from the arbitrary waveform generator (AWG). The 70 ps pulse duration $V_s$ generator passes through the low-noise amplifier (LNA) [96] with single-ended to differential conversion first, and then feeds into the DPC. The LNA has a bandwidth of 3 to 9 GHz and convert the single-end impulse to differential UWB pulses. Generated pulses are similar to the Gaussian doublet which has
Figure 5.8: Setup of the DPC test.

Figure 5.9: Measured differential input waveforms to the DPC prototype, generated by the LNA from a single-ended Gaussian-shape pulse.
Figure 5.10: Measured correlator outputs from the DPC prototype.
Figure 5.11: Measured DPC outputs with 200ps timing offset.

Figure 5.12: Measured DPC outputs with different templates.
Figure 5.13: Measured DPC outputs using same amplitude templates with opposite polarity.

a pulse duration of about 400 ps and a voltage swing of about 60 mV, as shown in Fig. 5.9. Two active delay lines are employed in the DPC. One is for the trigger distribution. An additional delay line is added in front to set the absolute time delay so that the input UWB pulses are aligned accurately with the trigger signal to the DPC (Fig. 5.4). The impulse generator and the DPC are synchronized by the signal source running at the pulse rate, which is 250 MHz in this test.

To verify the functionality of each tap, each single tap in the DPC is used to correlate with different part of a UWB pulse by sweeping the absolute time delay. Correct output polarity and amplitude are observed. The conversion gain shows a good tuning linearity with the change of reference bias current. Fig. 5.10 shows the differential correlation result for the pulse sequence. The differential correlator output amplitude is about 25 mV. The correlation output pulses show three phases during the operation: correlation, hold and reset. The hold phase maintains about 1 ns for the later VGA and ADC stages in a receiver, and the reset phase takes about 2 ns. The relatively long reset time is caused by the parasitic capacitance in shunt with the integration capacitors, which can be compensated by reducing the integration capacitance in an improved design later. Fig. 5.11 shows the correlator output when the input UWB pulses and trigger signals have timing offset. With
the 200ps timing offset, there is almost no correlation output waveform observed. Therefore, accurate timing and synchronization are critical for the correct detection using DPC. Fig. 5.12 shows the outputs when input UWB pulses are correlated with different local templates, local templates are constructed using tap 1 or tap 1, 4, 5 only, which only cover part of the UWB pulse. Since the pulse energy is not fully detected, output voltage level is smaller compared to the fully detected case using all tap 1-5. Template pulses with opposite polarity are also used while the template pulse amplitudes remain the same. The correlation results have very similar amplitudes but with opposite polarity, as shown in Fig. 5.13 These results verify that the built-in template pulse is reconfigurable.

5.4 Summary

A distributed pulsed correlator (DPC) circuit for impulse radio UWB receiver is demonstrated with a chip prototype implemented in a 0.18μm standard digital CMOS technology. By time-interleaving multiple pulsed multipliers, the 8-tap DPC prototype can detect the UWB pulse at 10GS/s rate with low power consumption which is 40pJ/b at 250Mbps data rate.
Chapter 6

Wideband Directional Coupler in Digital CMOS Technology

In this chapter, we present a wideband broad-side coupled CPW directional coupler using a commercial 0.18\( \mu \)m digital CMOS technology with low-resistivity epi substrate. The measurement results show 7 dB to 10 dB coupling and more than 10 dB directivity within 10-40 GHz.

6.1 Introduction

There have been strong interests in using silicon technologies for integrated circuits at millimeter-wave frequencies [97][98][56][99]. A major reason is the low cost associated silicon technologies. More compelling is silicon’s capability of integrating RF/microwave, analog, and digital circuits on a single chip, \textit{i.e.}, system-on-a-chip. It has become more feasible as recent progress in silicon technologies has pushed the cut-off frequency \((f_T)\) of NMOS transistors to over 150 GHz at 90 nm technology node and beyond 200GHz at 65 nm [9]. However, wide adoption of silicon technologies at frequencies beyond 10 GHz has been largely hindered by the lossy substrate, which results in large parasitic capacitance and high loss in on-chip passive devices. This is particularly problematic in digital CMOS technologies, in which a low-resistivity substrate \((\sim 10 \text{ m}\Omega \cdot \text{cm})\) with a thin epitaxial layer is usually used to avoid latch-up
and improve yield. Using bulk silicon substrate (\(\sim 10 \, \Omega \cdot \text{cm}\)) alleviates the problem and is widely used for RF applications under 10 GHz. Further increasing the substrate resistivity poses problems in wafer yield and wafer cost. On the other hand, the progress in silicon technologies leads to increasing number of interconnect metal layers, and thicker top metals. This has opened up opportunities to reduce the loss in on-chip passive devices through innovative electromagnetic design.

Furthermore, recent advances in silicon-based millimeter-wave ICs mainly focus on narrow-band applications [56][100]. There are even more challenges in the design and implementation of wideband MMICs using silicon technologies. One of them is the strong frequency dependency of on-chip passive device characteristics due to coupling to silicon substrate. For example, as frequency increases to millimeter-wave range, the spiral inductors may change the impedance from inductive to capacitive because of the self-resonance with parasitic coupling capacitance to silicon substrate. In this chapter, we use a directional coupler as an example to investigate how to achieve large bandwidth for passive devices at millimeter-wave frequencies using silicon technologies.

### 6.2 Microwave Directional Coupler

Directional couplers are important microwave passive devices for power division in various microwave circuits such as balanced amplifiers, balanced mixers, phase shifters, modulators, and measurement bridges. Branch-line couplers and hybrid ring couplers have been widely used as discrete devices or on printed circuit boards. Recently, a differential branch-line coupler has been implemented in a SiGe BiCMOS technology at 60 GHz to generate quadrature local oscillator signals [100]. However, branch-line couplers and hybrids usually consume large chip area [101]. Therefore, coupled-line couplers are more suitable for MMIC implementations because of their smaller footprint.

The requirements for the transmission lines in a directional coupler are low loss and convenience to achieve different impedance levels. Microstrip lines and coplanar waveguides (CPWs) can both be implemented in silicon technologies. For microstrip
Figure 6.1: CPW directional couplers (not to scale). (a) edge-coupled; (b) broadside-coupled.

lines, the signal line is usually built on the top metal layer, while the ground plane uses metal layers close to substrate. The achievable impedance level is usually low because of the small distance to the ground plane, and the minimum width limit for the signal line. CPWs can have both the signal and ground lines on the top metal layer, which usually is the thickest. The electromagnetic field is also moved further away from the lossy substrate. The impedance level of a CPW can be changed by adjusting the spacing between signal line and ground line. In addition, multiple metal layers can be stacked for the ground line to further reduce loss. Because of these reasons, coplanar waveguides are usually preferred for millimeter-wave circuits on silicon [97][55].

There are two major configurations for CPW directional couplers: edge-coupled [102], and broadside-coupled [103], as in Fig. 6.1. In silicon technologies, it is tempting to use the edge-coupled configuration since all transmission lines can then be constructed using the top metal layer, which is usually much thicker than lower metals. On the other hand, the gap between the two transmission lines in the edge-coupled configuration is limited by the design rule, which is significantly larger ($\sim 5 - 10\mu m$) for the thicker top metal layer. Hence, an interdigitated structure is usually needed in order to achieve enough coupling, which increases the chip area. In
the broadside-coupled configuration, the gap between different metal layers is quite small ($\sim 1 - 2\mu m$) while the metal traces can be quite wide, which makes strong coupling much easier to achieved. In addition, edge crowding effect increases the loss in the transmission lines, and largely offsets the benefits of using thicker metal for all transmission lines line. Thirdly, it is difficult for edge-coupled configuration to satisfy the metal density requirements mandated by chemical mechanical polishing (CMP) processes commonly used in silicon technologies because only one metal layer is placed within the area of coupled transmission lines. Instead, broadside-coupled configuration can have stacked multiple metal layers which is easier to satisfy the metal density requirements. Therefore, broadside-coupled configuration is well suited for strong coupling in silicon technologies. In this paper, we present our work on a wideband broadside-coupled directional coupler using multiple interconnect metal layers in silicon technologies.

### 6.3 Broadside Coupled Directional Coupler Design

The cross section of the coupler is shown in Fig. 6.2-a, which shows the structure of the multi-layer CPW. Two signal lines are built on M6 and M4. In order to have a strong coupling, the M4 line is placed right under the M6 line in a symmetric fashion. To achieve other coupling coefficients, asymmetric structure can also be used. The design target for the coupling coefficient is 6 dB, which implies the odd mode impedance is 28 Ohms and the even mode impedance is 87 Ohms, given 50 Ohms system impedance. Coupled multi-layer CPW lines with different configurations are simulated in 3D EM simulator HFSS [104], which can account for the effect of metal layer thickness. The design parameters for the coupling coefficient and impedance levels are the width of upper signal line, the width of lower signal line and the spacing between signal line and ground, since the distance between two signal lines are fixed. The dimensions to achieve desired impedance levels are also shown in Fig. 6.2-a. The line length of the directional coupler is designed to be 934 $\mu$m for a center frequency of 30 GHz. Because of the strong coupling between two signal lines, it is expected that this directional coupler would have a very wide bandwidth. The top view of the
Figure 6.2: Broadside-coupled CPW directional coupler in a digital CMOS process. (a) Cross section; (b) top view.
Figure 6.3: Electric fields of possibly excited modes: (a) dominant quasi-TEM mode; (b) coupled slot-line mode; (c) parasitic substrate mode; (d) parasitic waveguide mode.
whole directional coupler is shown in Fig. 6.2-b.

From EM simulations, it is found that extra modes might be excited. Four modes which can be excited from the port, are shown in Fig. 6.3. The corresponding phase factors are shown in Fig. 6.4. From this phase factor plot, we can see that the first three modes are propagating and the fourth one is an evanescent mode. The first mode is the desired propagating mode for such a transmission line structure. The second mode is the coupled slot-line mode, which might occur in any CPW lines at the presence of any discontinuity. To suppress this coupled slot-line mode, underpasses are connected between two ground lines to force them equal potential. The third one is a parasitic mode caused by the low resistivity silicon substrate. In order to suppress such a mode, many substrate contacts are added between ground lines and substrate to keep them equal potential. Two feed lines on M6 and M4 are also designed with the coupler with 50 Ohms impedance.

### 6.4 Measurement Results

The prototype coupler was fabricated in National Semiconductor’s 0.18μm standard digital CMOS technology with low-resistance epi substrate. The chip photo is
Figure 6.5: Die micrograph of the directional coupler.

Figure 6.6: Measured impedance levels of two feed lines.
Figure 6.7: Measured and simulated s-parameters of the coupler: (a) Through (S21) and Coupling (S31); (b) Matching (S11) and Isolation (S41).
Figure 6.8: Measured phase response of the coupler.

Figure 6.9: Measured directivity of the coupler.
shown in Fig. 6.5. The chip size is 1.4mm by 0.58mm. On the same die, two transmission lines with the same dimensions as feed lines which have 50 Ohms impedance are also fabricated for characterization purpose. One feed line is built on the top metal and the other is on Metal 4.

The measurement of the prototype coupler was performed in frequency domain up to 40 GHz via on-wafer probing. The measured impedance levels of two feed lines are shown in Fig. 6.6. They match with design value 50 Ohms well. This is very important for the coupler to have good terminations.

The measured and simulated s-parameters of the prototype coupler are both shown in Fig. 6.7 and Fig. 6.8 for both magnitude and phase response. The coupling coefficient is about 7 dB at 30 GHz, and it is flat within 20 GHz to 35 GHz. The -3 dB bandwidth can cover 10 GHz to 40 GHz. The return loss S11 is lower than -15 dB upto about 32 GHz and stays below -11 dB up to 40 GHz. The isolation (S41) is more than -20 dB to 30GHz and more than -16dB to 40GHz. The phase response is quite linear, and the phase difference between through port (S21) and coupled port (S31) is quite close to 90 degrees within the whole bandwidth. As in Fig. 6.9, the directivity is 24 dB at 10 GHz, and is more than 13 dB up to 30GHz. Until 40GHz, the directivity can still be more than 10 dB. The testing is performed up to 40 GHz; but as seen in Fig. 6.7.-a, the bandwidth is expected to extend beyond 40 GHz.

### 6.5 Summary

We have designed and fabricated a wideband broad-side coupled CPW directional coupler using a commercial 0.18\(\mu\)m digital CMOS technology with low-resistivity epi substrate. The measurement results show 7 dB to 10 dB coupling and more than 10 dB directivity within 10-40 GHz. There are several ways to further improve the design. For example, the layout of broadside coupler can be meandered or spiraled to reduce the size [105]. To achieve larger directivity, shunt capacitors which are available in digital CMOS technology can be used to compensate phase velocity difference between even and odd modes. We can also customize the relative lateral position of two signal lines in an asymmetric configuration [106] to have different coupling coefficients.
The proposed directional coupler can have a variety of applications in millimeter-wave integrated circuits for wireless communications, high-speed instrumentation, and radar systems.
Chapter 7

Future Work and Conclusions

7.1 Future Work

In this section, future work based on developed UWB pulse processing techniques is proposed. Several DPC based receiver architectures for different modulation schemes and the multipath channel will be discussed.

![DPC based IR-UWB receiver architecture for PPM.](image)

Figure 7.1: DPC based IR-UWB receiver architecture for PPM.
7.1.1 DPC Based IR-UWB Receiver Architectures

The DPC has been developed as an ultra-wideband pulse detection technique. The differential DPC prototype is already functional for the OOK modulation. In this section, we propose several other receiver architectures based on DPC for PPM and PSM modulated UWB pulses.

Fig. 7.1 shows the IR-UWB receiver architecture for PPM. In this architecture, multiple DPCs are used to detect possible locations of UWB pulses according to the modulation schemes selected. All timing information related to pulse positions is generated by the multi-phase clock generator. Multi-phase clock signal is essentially used to trigger all the DPCs to detect possible UWB pulses at different positions. Correlation outputs from all DPCs are then compared by the decision circuit to determine the exact position where the UWB pulse is located. So the information carried by the pulse position is demodulated.

The proposed receiver architecture for PSM is shown in Fig. 7.2. Because of the DPC’s reconfigurability, received orthogonal UWB pulses can be detected using a bank of DPCs which have different built-in local template pulses. The local template pulses are also orthogonal to each other, the same as transmitted/received orthogonal
pulses. In this case, the same trigger signal is used for all DPCs. Input UWB pulse is correlated with all the local template pulses at this moment. Correlation outputs from all DPCs are then compared to each other by the decision circuit to determine which local template pulse matches with the input UWB pulse. Thus, the information carried on pulse shapes is demodulated.

7.1.2 DPC Based IR-UWB RAKE Receiver Architecture

In the presence of multipath channel, the received UWB signal will be a sequence of transmitted UWB pulse and its delayed, weighted copies. The impulse response of the multipath channel is

\[ h(t) = \sum_{l=1}^{L_p} \alpha_l \delta(t - \tau_l) \]  

(7.1)

where \( \tau_l \) is the delay of signal path \( l \) and takes values in the continuous time-invariant model, \( \alpha_l \) is the gain of signal path \( l \), and \( L_p \) is the total number of paths.

Fig. 7.3 shows the proposed IR-UWB receiver architecture for the multipath channel. A bank of DPCs are utilized to detected received multiple signal copies through different signal path. So the total number of DPCs employed is determined by the number of paths \( L_p \). The amount of delay through different signal paths can be estimated by the channel estimation block. Correlation outputs are then weighted based on the estimation of signal path gain. After weighting, output signals are combined.
This essentially implements the RAKE receiver for UWB pulses.

7.2 Conclusions

This dissertation presents our studies on wideband/high-speed integrated circuits for ultra-wideband pulse generation, detection and filtering. We have demonstrated that CMOS technologies, despite the limitations in fundamental device characteristics, are capable of implementing wideband/high-speed circuits using distributed novel architecture and circuit techniques.

In Chapter 3, using distributed circuit technique for the filtering of ultra-wideband pulses, distributed amplifiers (DAs) with non-uniform filtering structures and distributed transversal filters (DTFs) were developed. Two DA prototypes with Butterworth and Chebyshev filtering were implemented using the concept of network synthesis method. A 5-tap DTF prototype with 50ps time resolution was implemented for sub-nanosecond pulse synthesis with 80ps rise time.

In Chapter 4, the distributed architecture was applied into the generation of ultra-wideband pulses using a newly-developed circuit, distributed waveform generator (DWG), with filtering and modulation functions. A DWG time-interleaves multiple pulse generators, and uses an on-chip transmission line for wideband pulse combining. The trading of circuit complexity for high-speed and low power consumption has been experimentally demonstrated using a 10-tap, 10GS/s single-polarity DWG prototype with digital pulse generators. For low-power IR-UWB applications, a 10-tap, 10GS/s, dual-polarity DWG with pulse position modulator was implemented as the transmitter with 3-9GHz bandwidth and 45pJ/pulse power efficiency.

The digital-assisted circuit technique was applied into the DWG and DTF design for dynamic range improvements on the pulse generation and filtering. To trade circuit complexity for accuracy, digital-to-analog converters (DAC) assisted pulse generators were incorporated into a 10.9GS/s DWG prototype to achieve more than 20dB dynamic range of pulse generation. Binary-weighted gain cell design was adopted in a DTF prototype for enhancing the dynamic range of wideband filtering.

In Chapter 5, the distributed architecture was also adopted in a new pulse circuit,
distributed pulsed correlator (DPC) for the detection of ultra-wideband pulses. A DPC time-interleaves multiple pulsed multipliers and has the built-in template pulse generator. An 8-tap, 10GS/s differential DPC prototype has been implemented as the RF front-end circuit of a IR-UWB receiver, which achieves 40pJ/b with 250Mbps data rate in the measurement. Receiver architectures based on DPC are also presented.

In Chapter 6, we presented a wideband broad-side coupled CPW directional coupler using a commercial 0.18μm digital CMOS technology with low-resistivity substrate. The measurement results show 7 dB to 10 dB coupling and more than 10 dB directivity within 10-40 GHz.

In Chapter 7, some receiver architectures based on the DPC have been proposed for the future work. The demodulation issues of PPM and PSM are discussed. IR-UWB RAKE receiver architecture is also presented.

Therefore, distributed architecture, distributed circuit techniques and digitally-assisted circuit techniques have become the main theme of this dissertation, with applications in ultra-wideband pulse generation, detection and filtering. It should be emphasized that the real strength of these techniques lies in the multi-level design from architectures, circuits to devices. Utilizing these innovative architectures and design techniques, the door to our never-ending quest for communication speed will be widely open.
Bibliography


[86] S. Liang, D. Huang, C. Ho, and H. Hong. A 10GS/s, 4-bit, 1.2V, design-for-testability ADC and DAC in 0.13μm CMOS technology.


